

Optimizing MOSFET Gate Drive Voltage

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The topic of MOSFET gate drive has been well documented by various sources. Most publications related to power supply applications highlight switching properties of the MOSFET and various methods that can be used to turn the devices on and off as efficiently as possible. One aspect often overlooked is the issue of gate drive voltage amplitude and the role it can play in overall power converter efficiency. This article addresses some of the trade-offs that exist when considering one gate drive voltage level versus another. Although these principles can apply to most switching power supply topologies, this article uses the synchronous buck as an application example. Graphs showing frequency and load current trade-offs present general MOSFET power loss equations. For discrete MOSFET gate drive circuits, driver ICs and PWM controllers, this methodology can apply to any power supply application with the capability to vary the gate drive voltage amplitude.

Introduction

Power supply designers can sometimes gain additional efficiency by properly matching the gate drive voltage with the MOSFETs being driven. Driving a MOSFET gate with a higher voltage, results in a lower associated on-resistance, $R_{ds(ON)}$, up to a particular point of diminishing return. This can be extremely beneficial to low voltage high current VRM designs and control-driven synchronous rectifiers found in many high current isolated power supply applications. In synchronous buck power applications, lowering the MOSFET on-resistance is especially critical for the synchronous rectifier, since in most cases the power loss due to the freewheeling current through the MOSFET channel resistance is the highest single contributor to total dissipated power. There are, however, additional factors to consider.

Higher gate drive voltage levels place additional charge into the gate-to-source junction of the MOSFET, resulting in increased losses within the MOSFET driver stage. In addition, a higher gate charge requirement will produce longer rise and fall times, which impact switching losses in the high-side MOSFET of a synchronous buck converter. To increase efficiency the applied voltage should drive the MOSFET gates such that the added gate charge and switching losses are less than the power savings gained by lowering $R_{ds(ON)}$. For example, taking on an additional 0.5 W of power dissipated in the high-side MOSFET may be acceptable when 1 W of power is saved in the synchronous MOSFET.

Definition of Symbols and Abbreviations

The following list of symbols and abbreviations are used throughout the application example of this article.

D	Duty Cycle
F_{sw}	Switching Frequency
G1	Control MOSFET Gate Drive
G2	Synchronous Rectifier MOSFET Gate Drive
$I_{G(sink)}$	Driver Sink Current
$I_{G(source)}$	Driver Source Current
I_{OUT}	Output Load Current
L_{LUMP}	Driver to MOSFET Parasitic Inductance
P_{bd}	Synchronous Rectifier MOSFET Body-Diode Power Loss
P_c	MOSFET Conduction Power Loss
P_d	Total Dissipated Power (G1, Q1, G2, Q2)
P_{out}	MOSFET Output Capacitance Loss
P_{RR}	Synchronous Rectifier MOSFET Body-Diode Reverse Recovery Power Loss
P_{SW}	MOSFET Switching Loss
Q_g	Total Gate Charge
Q_{RR}	Body-Diode Reverse Recovery Charge
Q1	Control MOSFET
Q2	Synchronous Rectifier MOSFET
$R_{ds(ON)}$	MOSFET Drain-to-Source On Resistance
R_g	MOSFET External Discrete Gate Resistance
R_{gi}	MOSFET Internal Gate Resistance
$R_{G1(sink)}$	G1 Driver Sink Resistance
$R_{G1(source)}$	G1 Driver Source Resistance
$R_{G2(sink)}$	G2 Driver Sink Resistance
$R_{G2(source)}$	G2 Driver Source Resistance
t_{BDF}	MOSFET Body-Diode Conduction Time, Switch Node Falling
t_{BDR}	MOSFET Body-Diode Conduction Time, Switch Node Rising
t_f	MOSFET Turn Off Fall Time
t_r	MOSFET Turn On Rise Time
V_F	MOSFET Body-Diode Forward Voltage Drop
V_{GS}	Gate-to-Source Voltage
V_{IN}	Input Voltage
V_{TH}	MOSFET Turn On Threshold Voltage
V_{OUT}	Output Voltage
$\Delta\eta$	Change in Overall Efficiency

Gate Drive Voltage Considerations

Driving the gates of control MOSFET Q1 and synchronous MOSFET Q2 (see Fig. 1) with one voltage level V_s . another requires careful consideration. The need for additional discrete components, impact to the PCB routing, and the requirement of optimal drive voltage amplitudes that may or may not be readily available, are all trade-offs to weigh against the potential efficiency savings from possibly lowering the MOSFET $R_{ds(ON)}$.

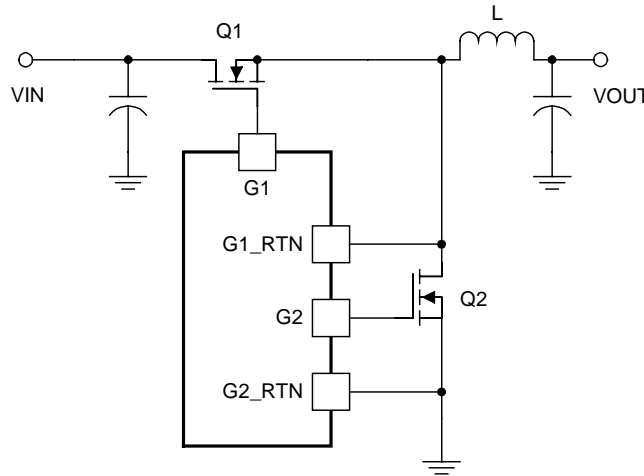


Fig. 1: Synchronous Buck Power and Driver Stage

As an example, consider the following analysis using arbitrary devices for the control MOSFET and synchronous rectifier MOSFET. In order to weigh the benefit of one gate-source voltage (V_{GS}) Vs. another, the $R_{ds(ON)}$ Vs. gate drive voltage and gate drive voltage Vs. gate charge curves for each MOSFET must be carefully looked at. Fig. 2 through Fig. 4 show typical MOSFET performance characteristics found in most manufacturers' data sheets and will be used as a basis for the following application example.

Q1 - Control MOSFET

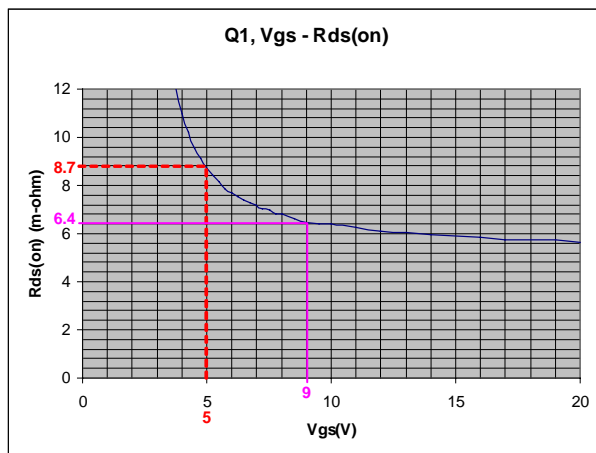


Fig. 2: Q1 - Vgs Vs. Rds

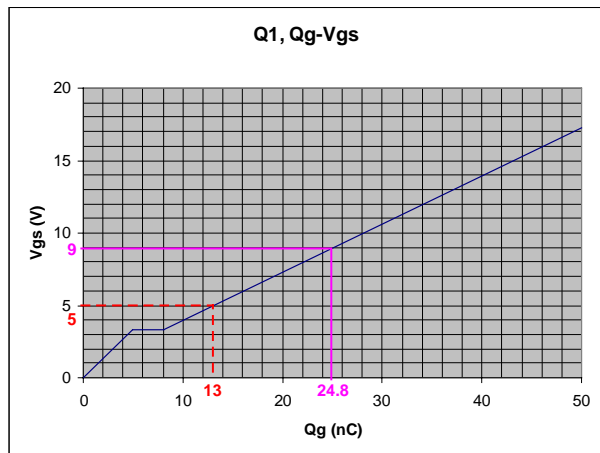


Fig. 3: Q1 - Qg Vs. Vgs

Fig. 2 highlights the $R_{ds(ON)}$ values for $V_{GS} = 5\text{ V}$ and 9 V for the control MOSFET, Q1 but because it is more prone to switching loss it is normally selected based on lower gate charge, with secondary consideration given to $R_{ds(ON)}$. For $V_{GS} = 5\text{ V}$, $R_{ds(ON)} = 8.7\text{ m}\Omega$, and for $V_{GS} = 9\text{ V}$, $R_{ds(ON)} = 6.4\text{ m}\Omega$. Fig. 2 shows the impact on gate charge increasing V_{GS} from 5 V to 9 V . For $V_{GS} = 5\text{ V}$, $Q_g = 13\text{ nC}$, and for $V_{GS} = 9\text{ V}$, $Q_g = 24.8\text{ nC}$. Table 1 summarizes the results.

Q2 – Synchronous Rectifier MOSFET

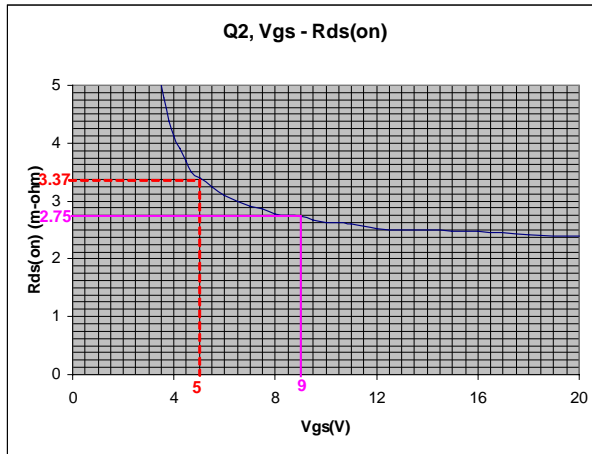


Fig. 4: Q2 - Vgs Vs. Rds

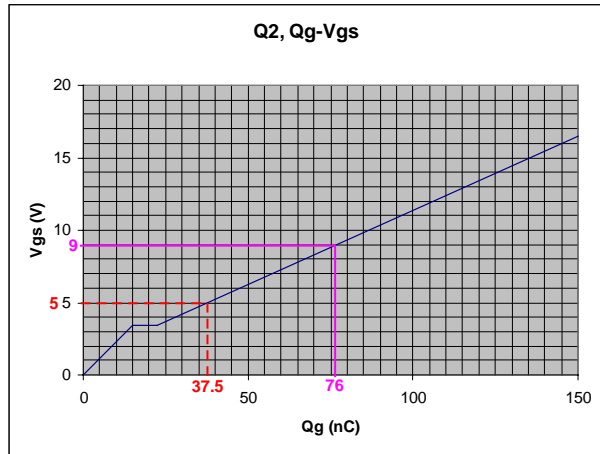


Fig. 5: Q2 - Qg Vs. Vgs

Fig. 4 highlights the $R_{ds(ON)}$ values for $V_{GS} = 5\text{ V}$ and 9 V for the synchronous rectifier MOSFET, Q2. Since it is more prone to conduction loss, Q2 is selected based upon lowest possible $R_{ds(ON)}$, with secondary consideration given to gate charge. For $V_{GS} = 5\text{ V}$, $R_{ds(ON)} = 3.37\text{ m}\Omega$, and for 9 V , $R_{ds(ON)} = 2.75\text{ m}\Omega$. Fig. 5, shows the impact on gate charge for increasing V_{GS} from 5 V to 9 V . For $V_{GS} = 5\text{ V}$, $Q_g = 37.5\text{ nC}$, and for $V_{GS} = 9\text{ V}$, $Q_g = 76\text{ nC}$. MOSFET parameters for each case of V_{GS} are summarized in Table 1.

V_{GS} (V)	$R_{ds(ON)}$ (m Ω)	Q_g (nC)	C_{oss} (pF)	R_{gi} (Ω)	V_{th} (V)
Q1 – Control MOSFET					
5	8.7	13	400	0.5	2
9	6.4	24.8	400	0.5	2
Q2 – Synchronous Rectifier MOSFET					
5	3.37	37.5	1200	0.5	2
9	2.75	76	1200	0.5	2

Table 1: MOSFET Parameters for Varying V_{GS}

Depending upon the maximum load current, the lower $R_{ds(ON)}$ resulting from higher V_{GS} will result in lower conduction losses up to some cut-off frequency where switching losses will begin to dominate. At higher frequencies, where switching losses dominate, the lower gate charge resulting from lower V_{GS} will be preferred. At lower frequencies, where conduction losses

dominate, the lower $R_{ds(ON)}$ resulting from higher V_{GS} will be preferred. In terms of increasing efficiency, the best choice may be to drive the control MOSFET with a lower V_{GS} to minimize switching losses, and the synchronous rectifier with higher V_{GS} to lower conduction loss. However, since most synchronous buck MOSFET drivers do not offer the option of independently driving the control gate and synchronous gate with different voltages, this may not be a practical solution.

The following application example will compare the efficiency results for two cases of V_{GS} . For simplicity, the same amplitude V_{GS} will be used for the control MOSFET and synchronous MOSFET for each case.

APPLICATION EXAMPLE

Given the following specifications:

- $V_{IN} = 5\text{ V}$
- $V_{OUT} = 1.8\text{ V}$
- $I_{OUT} = 20\text{ A}$
- $D = 0.36$
- $F_{sw} = 200\text{ kHz}$
- $R_g = 0\ \Omega$
- $L_{LUMP} = 50\text{ nH}$

MOSFET Driver Characteristics:

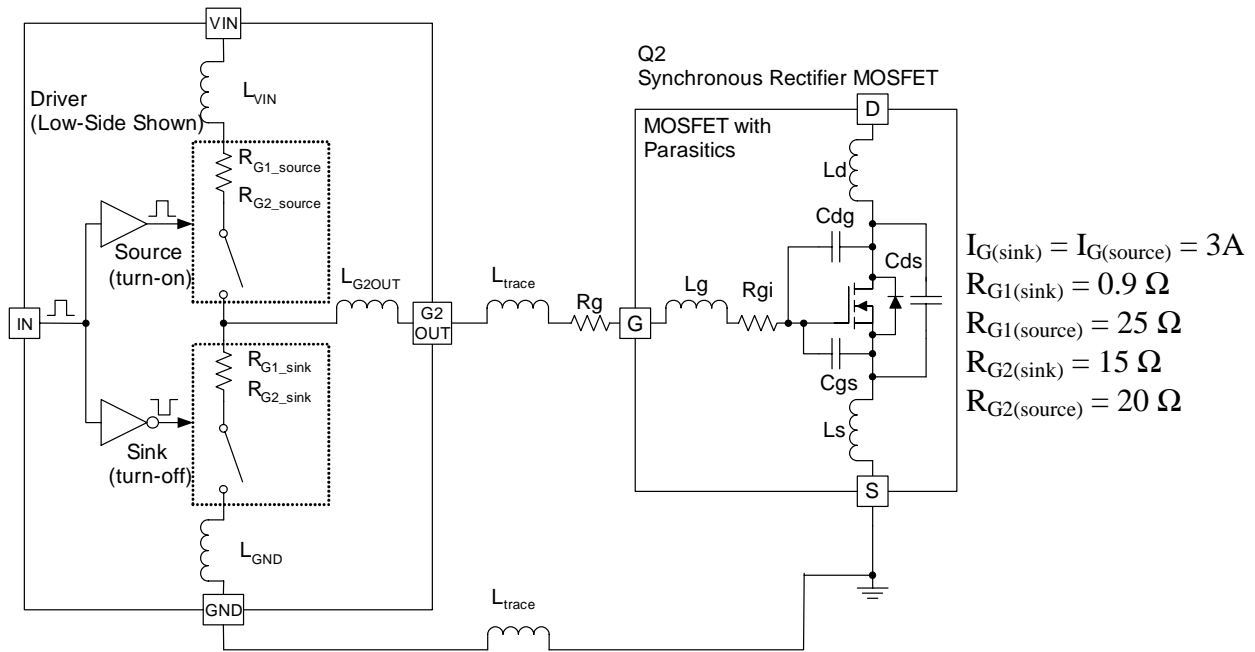


Fig. 6: Low-Side Driver and MOSFET Parasitic Model

Fig. 6 shows a representative model of the parasitic elements that can impact switching power supply performance. For simplicity only the low-side synchronous rectifier MOSFET and driver stage are shown. The resistances associated with the driver sink and source impedances quite often are not the same value and should be specified in a manufacturer's data sheet. It is also important to mention the effect of parasitic inductance between the driver and the MOSFET. At higher-frequency operation this inductance can limit the gate current trying to charge the MOSFET input capacitance. Eq. 2 verifies that this will result in slower rise and fall times and additional switching losses. The total lumped parasitic inductance, L_{LUMP} , for this example is assumed to be 50 nH and consists (Fig. 6, again) mostly of internal lead inductance associated with the MOSFET and driver package. Since the designer has no control over these parameters the only component of parasitic inductance that can be controlled is trace inductance, L_{trace} , so minimizing the length of trace between the driver and the MOSFET, as well as running a short and wide gate trace directly over a ground plane, will reduce parasitic trace inductance.

Control MOSFET Power Loss Calculations:

$$P_c = I_{out}^2 \times R_{ds(ON)} \times D \quad \text{Eq. 1}$$

$$P_{sw} = \frac{1}{2} \times V_{IN} \times I_{out} \times (t_r + t_f) \times F_{sw} \quad \text{Eq. 2}$$

where, $t_r \approx t_f$, and is approximated by:

$$t_r = t_f = \frac{Q_G}{I_G} + \frac{L_{LUMP} \times I_G}{V_{GS} - V_{th}} \quad \text{Eq. 3}$$

$$P_{out} = \frac{1}{2} \times \frac{4}{3} \times C_{oss} \times V_{IN}^2 \times F_{sw} \quad \text{Eq. 4}$$

High Side Driver Power Loss:

Since the sink and source resistances of the driver are so much greater than the MOSFET's internal gate resistance, most of the switch loss associated with charging and discharging the MOSFET gate is dissipated in the driver IC.

$$P_{G1} = Q_g \times V_{GS} \times F_{sw} \times \left(\frac{R_{G1_sink}}{R_{G1_sink} + R_g + R_{gi}} + \frac{R_{G1_source}}{R_{G1_source} + R_g + R_{gi}} \right) \quad \text{Eq. 5}$$

Eqs. 1 - 5 can approximate total losses for the control MOSFET and driver for each case of V_{GS} .

Synchronous Rectifier MOSFET Power Loss Calculations:

For simplification of calculations, assume the following body-diode characteristics:

- $t_{BDR} + t_{BDF} = 10 \text{ ns}$
- $Q_{RR} = 48 \text{ nC}$
- $V_F = 1 \text{ V}$

$$P_{bd} = V_F \times I_{out} \times F_{sw} \times (t_{BDR} + t_{BDF}) \quad \text{Eq. 6}$$

$$P_c = I_{out}^2 \times R_{ds(ON)} \times (1 - D) \quad \text{Eq. 7}$$

$$P_{RR} = Q_{RR} \times V_{IN} \times F_{sw} \quad \text{Eq. 8}$$

$$P_{SW} = 0 \quad \text{Eq. 9}$$

$$P_{out} = 0 \quad \text{Eq. 10}$$

Low Side Driver Power Loss:

$$P_{G2} = Q_g \times V_{GS} \times F_{sw} \times \left(\frac{R_{G2_sink}}{R_{G2_sink} + R_g + R_{gi}} + \frac{R_{G2_source}}{R_{G2_source} + R_g + R_{gi}} \right) \quad \text{Eq. 11}$$

Using Eqs. 6 - 11, the designer can approximate the total losses for the synchronous rectifier MOSFET and driver for each case of V_{GS} . Since many of the individual losses represented by all eleven equations are frequency dependant, a spreadsheet was designed to calculate and plot the total losses associated with the upper control MOSFET and lower synchronous MOSFET V_s frequency for each case of V_{GS} . A spreadsheet or MathCAD can make it easy to determine the effect of varying the V_{GS} value.

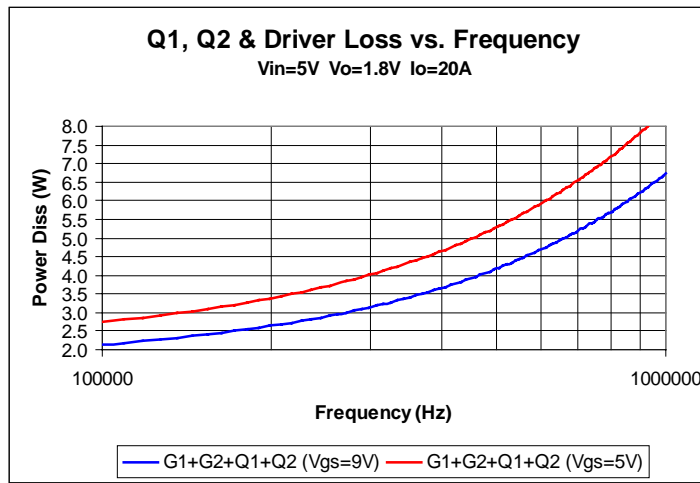


Fig. 7: P_{diss} Vs. Frequency

Fig. 7 shows equations 1 - 11 plotted against varying frequency (100 kHz to 1 MHz) for each case of V_{GS} . Although these graphs can be generated at any output load current of interest, the results of Fig. 7 are shown at $I_{OUT(MAX)} = 20$ A, which is the point where rising MOSFET junction temperatures benefit most from higher efficiency. For $I_{OUT} = 20$ A, it is clear that $V_{GS} = 9$ V results in significantly less dissipated power over all frequencies of interest.

Having calculated the total dissipated power for each case of V_{GS} , and knowing the maximum output power, the graph of Fig. 8 is developed using Eq. 12.

$$\Delta\eta = \left[\frac{\pm P_{OUT(MAX)} \times (P_{d(9V)} - P_{d(5V)})}{(P_{OUT(MAX)} + P_{d(5V)}) \times (P_{OUT(MAX)} + P_{d(9V)})} \right] \times 100\% \quad \text{Eq. 12}$$

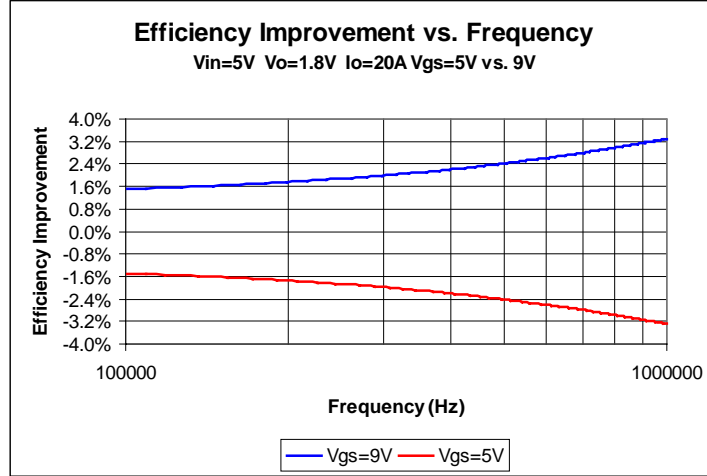


Fig. 8: Efficiency Improvement Vs. Frequency

In addition to the driver and MOSFET effects, the power stage components must also be considered when selecting the optimal switching frequency. Since analyzing the power stage frequency effects are beyond the scope of this example, it is assumed that 200 kHz is a good trade-off between optimizing the MOSFET and gate drive circuitry and maintaining a fairly high frequency to minimize the size of the passive components in the power stage. The graph of Fig. 8 shows an efficiency increase of approximately 1.7% at 200 kHz, for $V_{GS} = 9V$ and $I_{OUT} = 20A$.

Selecting a switching frequency of 200 kHz, it would be helpful to know what effect V_{GS} will have over the entire load range at the selected frequency. Eqs. 1 - 11 can next be plotted Vs. load current at a fixed 200 kHz frequency.

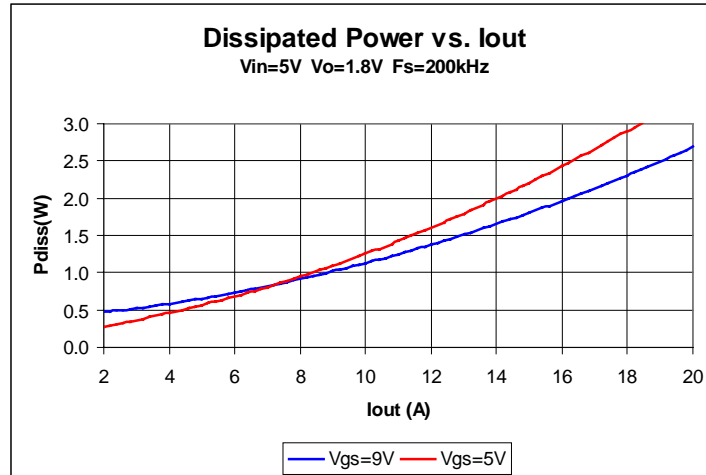


Fig. 9: P_{diss} Vs Load Current

Fig. 9 shows the effects of power dissipation Vs. load current for $V_{GS} = 5\text{ V}$ and $V_{GS} = 9\text{ V}$ at a fixed 200 kHz frequency.

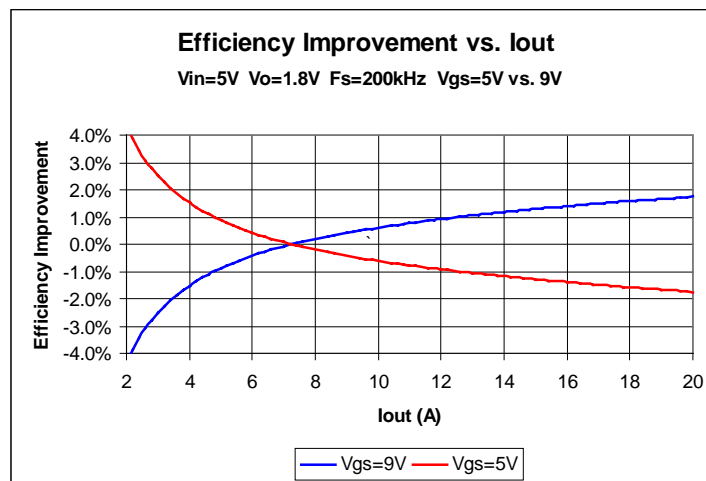


Fig. 10: Efficiency Improvement Vs. Load Current

As expected Fig. 10 shows a 1.7% efficiency increase for $V_{GS} = 9\text{ V}$ at $I_{OUT} = 20\text{ A}$. However, at I_{OUT} less than 7 A it results in an efficiency loss compared to $V_{GS} = 5\text{ V}$. For I_{OUT} less than 7 A, the efficiency improvement resulting from lower conduction loss has less effect, evidenced by Eqs. 1 and 7 as frequency-dependant losses begin to dominate over current-dependant (conduction) losses, so a lower $V_{GS} = 5\text{ V}$, and a lower overall gate charge, is preferred.

It is interesting to note that by iterating through this graphical process we can optimize the combination of V_{GS} and switching frequency. In this example, for instance, using $V_{GS} = 9\text{ V}$ at a frequency of 200 kHz we gain 1.7% efficiency at maximum output current, at the cost of lower efficiency at lighter load current. Conversely, using $V_{GS} = 5\text{ V}$ at 200 kHz would result in higher efficiency just below the mid range of load current, but a lower efficiency at higher load current.

Calculations

Following are the detailed calculations used to generate the graphs in Figs. 7 - 10.

Control MOSFET, $V_{GS} = 5\text{ V}$:

$$P_{c(5V)} = 20A^2 \times 8.7 \times 10^{-3} \Omega \times 0.36 = 1.253W \quad \text{Eq. 13}$$

$$t_{r(5V)} = t_{f(5V)} = \frac{13 \times 10^{-9} C}{3A} + \frac{50 \times 10^{-9} H \times 3A}{5V - 2V} = 54.3 \times 10^{-9} s \quad \text{Eq. 14}$$

$$P_{SW(5V)} = \frac{1}{2} \times 5V \times 20A \times (54.3 \times 10^{-9} s + 54.3 \times 10^{-9} s) \times (200 \times 10^3 \text{ Hz}) = 1.09W \quad \text{Eq. 15}$$

$$P_{out(5V)} = \frac{1}{2} \times \frac{4}{3} \times 400 \times 10^{-12} F \times 5V \times 200 \times 10^3 \text{ Hz} = 0.27mW \quad \text{Eq. 16}$$

And the power dissipated in the driver IC at $V_{GS} = 5V$ is:

$$P_{G1(5V)} = 13 \times 10^{-9} C \times 5V \times 200 \times 10^3 \text{ Hz} \times \left(\frac{0.9\Omega}{0.9\Omega + 0 + 0.5\Omega} + \frac{25\Omega}{25\Omega + 0 + 0.5\Omega} \right) = 21.1mW \quad \text{Eq. 17}$$

The total power loss of the upper control MOSFET and the gate driver IC is simply the sum of all the losses given by Eqs. 13 through 17:

$$P_{G1_TOTAL(5V)} = 1.253W + 1.09W + 0.27 \times 10^{-3} W + 21.1 \times 10^{-3} W = 2.36W \quad \text{Eq. 18}$$

Control MOSFET, $V_{GS} = 9V$:

$$P_{c(9V)} = 20A^2 \times 6.4 \times 10^{-3} \Omega \times 0.36 = 0.922W \quad \text{Eq. 19}$$

$$t_{r(9V)} = t_{f(9V)} = \frac{24.8 \times 10^{-9} C}{3A} + \frac{50 \times 10^{-9} H \times 3A}{9V - 2V} = 30 \times 10^{-9} s \quad \text{Eq. 20}$$

$$P_{SW(9V)} = \frac{1}{2} \times 5V \times 20A \times (30 \times 10^{-9} s + 30 \times 10^{-9} s) \times (200 \times 10^3 \text{ Hz}) = 0.6W \quad \text{Eq. 21}$$

$$P_{out(9V)} = \frac{1}{2} \times \frac{4}{3} \times 400 \times 10^{-12} F \times 5V \times 200 \times 10^3 \text{ Hz} = 0.27mW \quad \text{Eq. 22}$$

And the power dissipated in the driver IC at $V_{GS} = 9V$ is:

$$P_{G1(9V)} = 24.8 \times 10^{-9} C \times 9V \times 200 \times 10^3 \text{ Hz} \times \left(\frac{0.9\Omega}{0.9\Omega + 0 + 0.5\Omega} + \frac{25\Omega}{25\Omega + 0 + 0.5\Omega} \right) = 72.46mW \quad \text{Eq. 23}$$

The total power loss of the upper control MOSFET and the gate driver IC is simply the sum of all the losses given by Eqs. 19 through 23.

$$P_{G1_TOTAL(9V)} = 0.922W + 0.6W + 0.27 \times 10^{-3}W + 72.46 \times 10^{-3}W = 1.595W \quad \text{Eq. 24}$$

Synchronous Rectifier MOSFET, $V_{GS} = 5$ V:

$$P_{bd(5V)} = 1V \times 20A \times 200 \times 10^3 Hz \times (10 \times 10^{-9} s) = 40 \times 10^{-3}W \quad \text{Eq. 25}$$

$$P_{c(5V)} = 20A^2 \times 3.37 \times 10^{-3} \Omega \times (1 - 0.36) = 0.863W \quad \text{Eq. 26}$$

$$P_{RR(5V)} = 37.5 \times 10^{-9} C \times 5V \times 200 \times 10^3 Hz = 37.5 \times 10^{-3}W \quad \text{Eq. 27}$$

And the power dissipated in the driver IC at $V_{GS} = 5$ V is:

$$P_{G2(5V)} = 37.5 \times 10^{-9} C \times 5V \times 200 \times 10^3 Hz \times \left(\frac{15\Omega}{15\Omega + 0 + 0.5\Omega} + \frac{20\Omega}{20\Omega + 0 + 0.5\Omega} \right) = 72.88 \times 10^{-3}W \quad \text{Eq. 28}$$

The total power loss of the synchronous rectifier MOSFET and the gate driver IC is simply the sum of all the losses given by Eqs. 25 through 28.

$$P_{G2_TOTAL(5V)} = 40 \times 10^{-3}W + 0.863W + 37.5 \times 10^{-3}W + 72.88 \times 10^{-3}W = 1.014W \quad \text{Eq. 29}$$

Synchronous Rectifier MOSFET, $V_{GS} = 9$ V:

$$P_{bd(9V)} = 1V \times 20A \times 200 \times 10^3 Hz \times (10 \times 10^{-9} s) = 40 \times 10^{-3}W \quad \text{Eq. 30}$$

$$P_{c(9V)} = 20A^2 \times 2.75 \times 10^{-3} \Omega \times (1 - 0.36) = 704 \times 10^{-3}W \quad \text{Eq. 31}$$

$$P_{RR(9V)} = 76 \times 10^{-9} C \times 5V \times 200 \times 10^3 Hz = 76 \times 10^{-3}W \quad \text{Eq. 32}$$

And the power dissipated in the driver IC at $V_{GS} = 9$ V is:

$$P_{G2(9V)} = 76 \times 10^{-9} C \times 9V \times 200 \times 10^3 Hz \times \left(\frac{15\Omega}{15\Omega + 0 + 0.5\Omega} + \frac{20\Omega}{20\Omega + 0 + 0.5\Omega} \right) = 265.85 \times 10^{-3}W \quad \text{Eq. 33}$$

The total power loss of the synchronous rectifier MOSFET and the gate driver IC is simply the sum of all the losses given by Eqs. 30 through 33.

$$P_{G2_TOTAL(9V)} = 40 \times 10^{-3}W + 704 \times 10^{-3}W + 76 \times 10^{-3}W + 265.85 \times 10^{-3}W = 1.086W \quad \text{Eq. 34}$$

Results from the application example are summarized in Table 2:

V_{GS}	Q1 (Control MOSFET)	Q2 (SR MOSFET)	Driver IC (G1)	Driver IC (G2)	Total Power Loss (MOSFETs + Driver IC)	$\Delta\eta$
5 V	2.34 W	0.941 W	21.1 mW	72.88 mW	3.375 W	N/A
9 V	1.52 W	0.820 W	72.46 mW	265.85 mW	2.678 W	1.65%

Table 2: $F=200$ kHz, $I_{OUT}=20$ A, Power Dissipation Summary for Varying V_{GS}

For $F_{sw} = 200$ kHz and $I_{OUT} = 20$ A, driving Q1 and Q2 with $V_{GS} = 9$ V as opposed to $V_{GS} = 5$ V results in an overall efficiency improvement of nearly 1.7% as shown in

Table. The results shown in

Table closely agree with the calculated graphical results in Figs. 7 - 10. For this example a significant overall efficiency improvement can be gained by driving Q1 and Q2 with $V_{GS} = 9$ V, at the trade-off of slightly lower efficiencies below $I_{OUT} = 7$ A. The total losses for Q1 and Q2 given in

Table seem reasonable; however the thermal impedances of each MOSFET package should also be considered to make sure that junction temperatures are within rated limits. If junction temperatures are not being exceeded by chosen design constraints, it may be possible to further increase the switching frequency.

Conclusions

Using a given set of design parameters for a synchronous buck power stage, a full-load efficiency gain of up to 1.7% can be realized when the MOSFET gates are driven at 9 V as opposed to 5 V. For this example conduction losses were dominant at load currents greater than 7 A. For load currents less than 7 A switching losses were dominant and efficiency was shown to actually decrease by up to 4%. In summary, higher light load efficiency could be expected for $V_{GS} = 5$ V, and higher full load efficiency was shown at $V_{GS} = 9$ V. When considering what level of V_{GS} to design for, examining the MOSFET power loss equations graphically can offer better insight as to where the benefits lie when frequency and output current are varied.

Given the choice, what is the optimal gate drive voltage amplitude for driving a switching MOSFET in a power supply application? The answer is not always clear but with the aid of a spreadsheet or MATHCAD, the designer can make a fair comparison to graphically examine the trade-offs and potential benefits.

References

Power Supply Design Seminar SEM-1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP169 <http://focus.ti.com/lit/ml/slup169/slup169.pdf>

Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits, by Bill Andreyckak, Texas Instruments Literature No. SLUA105

Power Supply Design Seminar SEM-1500 Topic 5: *Under the Hood of Low-Voltage DC/DC Converters*, by Brian Lynch and Kurt Hesse, Texas Instruments Literature No. SLUP206 <http://focus.ti.com/lit/ml/slup206/slup206.pdf>

Estimating MOSFET Switching Losses Means Higher Performance Buck Converters, by Peter Markowski, PlanetAnalog.com, December 18, 2002

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