

Speed-up Start-up in PFC Pre-Regulators

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Editor's Note: For best legibility the complete PFC application circuit (referred as Fig. 1) is reproduced on the last page of this TechNote. Readers needing the circuit as a separate file can download it at <http://www.analogZONE.com/pwrt1101a.pdf> or [pwrt1101a.jpg](http://www.analogZONE.com/pwrt1101a.jpg).

Power Factor Corrected (PFC) Pre-regulator boost converters are generally compensated with a slow voltage loop (Fig. 2) to reduce input current total harmonic distortion (THD). In most applications, the PFC Pre-regulator's small signal voltage loop is designed to cross over at less than one seventeenth of the line frequency. In an offline converter with a 60-Hz line frequency, the voltage loop would crossover at less than 10 Hz. Fig. 3 shows the typical voltage loop frequency response of PFC pre-regulator operating off a 60-Hz line.

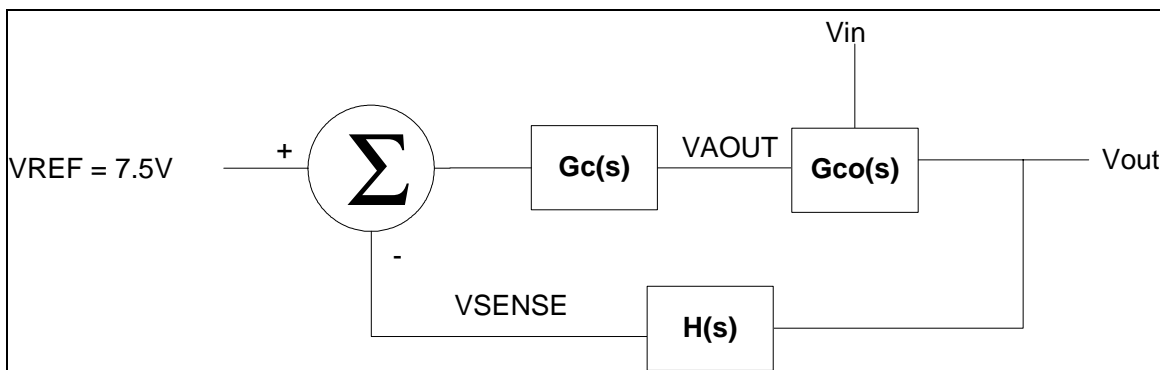


Fig. 2: Voltage Loop Control Block Diagram

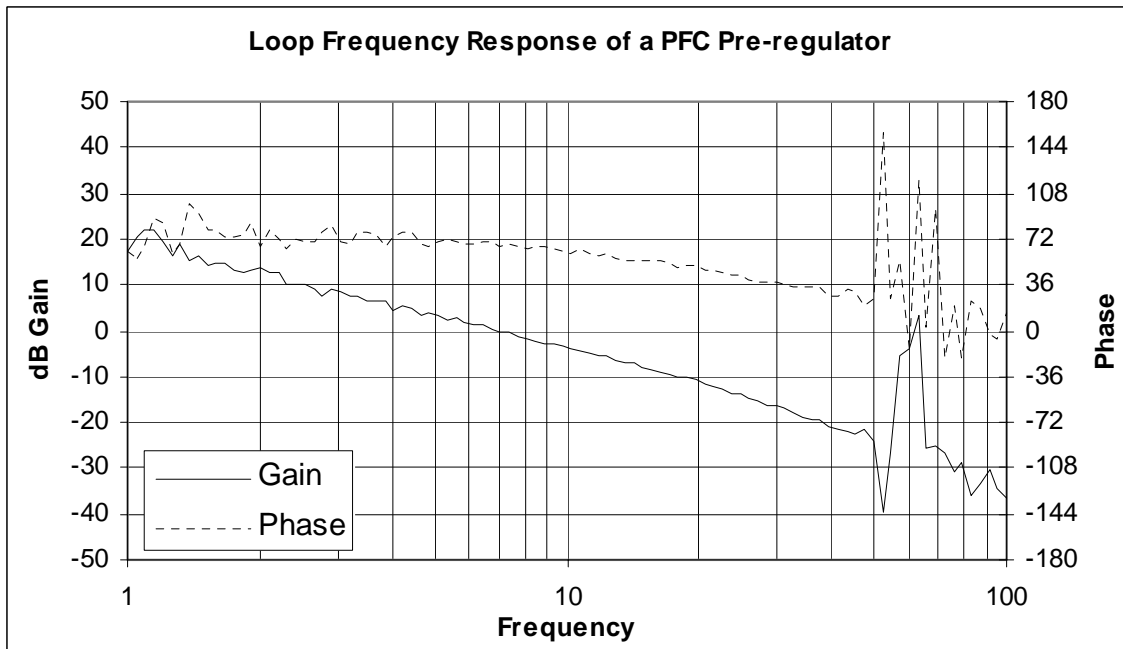


Fig. 3: Voltage Loop Frequency Response

The small-signal bandwidth of the voltage loop presents a challenge for the power supply designer. The fastest the loop can respond to a small signal change is roughly 100 ms. For a large signal change such as start-up it could take hundreds of milliseconds for the loop to respond. During start-up, the boost voltage would overshoot because the voltage loop is not fast enough to correct for the large signal transient. To prevent overshoot during power up, a power supply designer would have to bring up the output voltage slowly. This is generally done with a soft-start (SS) function that is provided in most modern pulse width modulator (PWM) controllers.

Review of a Typical PFC Application:

The PFC pre-regulator is typically part of a two-stage power system. The first is a boost converter, where the input current is shaped through average current-mode control to achieve near unity power factor. For the boost converter to work correctly it requires an output voltage higher than the input and a second stage is required to step this large voltage down to a usable output voltage.

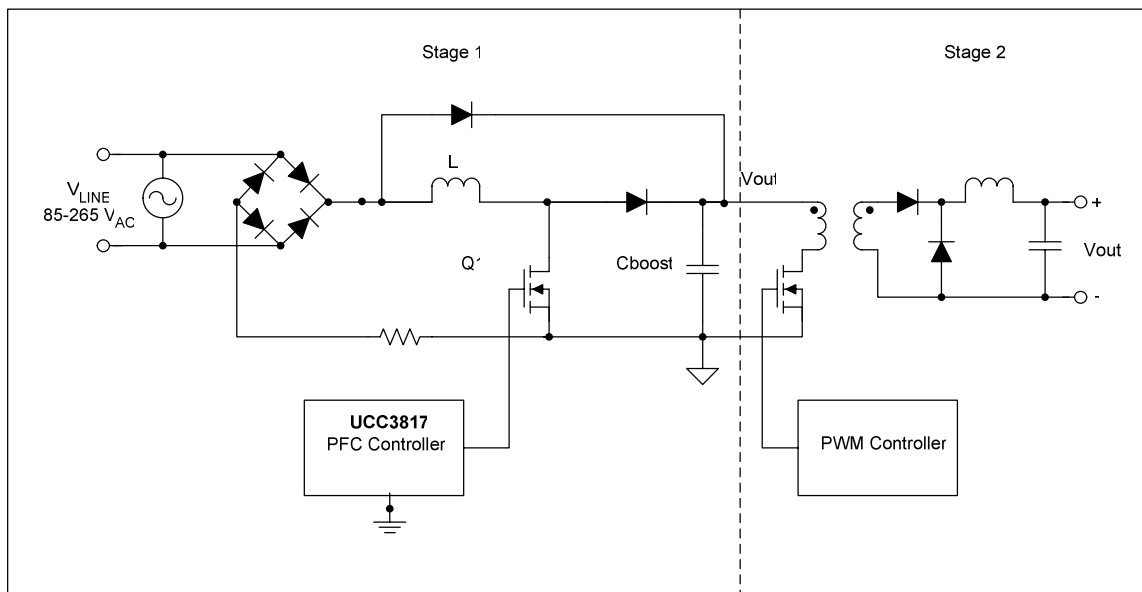


Fig. 4: Typical Two-Stage System with PFC Pre-regulator

The schematic in Fig. 1 (see last page) shows a PFC pre-regulator that was designed to operate off a universal line voltage (ie 85 Vrms to 265 Vrms) with a regulated 385 V, 250 W dc output. The second power stage that would be downstream from this pre-regulator typically is designed to operate with an input voltage as low as 75% of the pre-regulator's output to handle "brownout" conditions.

Problem

In some applications, the design requires a fast start-up and bringing up the boost voltage slowly is not an option. A major problem with speeding up the soft start is the boost voltage will overshoot: electrically stressing the boost capacitor (C12) of Fig. 1.

The circuit in Fig. 1 needed to be designed to soft-start within 300 ms. The design requirement was that the boost voltage be within 75% of its targeted output voltage within 300 ms. The waveform in Fig. 5 shows the startup characteristics of this design. CH1 is the output voltage (Vout), CH2 is the voltage amplifier output (VAOUT) and CH3 is the soft-start (SS) voltage. CH4 is the gate drive signal from the DRVOUT pin of the UCC3817 that controls the boost switch Q1.

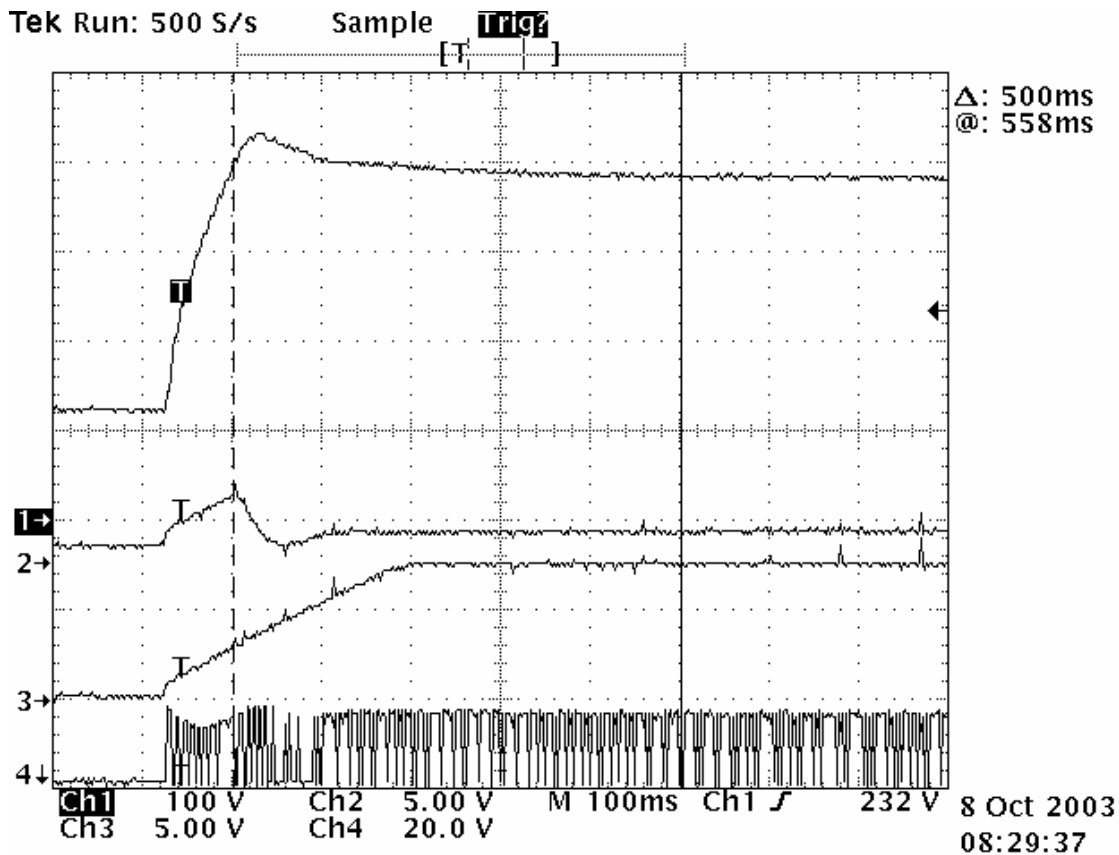


Fig. 5: Typical Start Behavior For A PFC Pre-Regulator

The power supply was designed to have the output voltage (Vout) tracking the soft-start (SS) voltage at pin 13 of the UCC3817 PFC controller. However, because the voltage loop of the converter was slow, it did not track SS and overshoot during power-up and peaked at roughly 435 V, an overshoot of approximately 13%. From the waveforms in Fig. 3 it can be observed that the soft start function of the control IC was working correctly. The output voltage and VAOUT tracked soft-start until the output reaches 385 V. Once VOUT goes above 385 V, the voltage amplifier output goes low demanding a minimum duty cycle, but the voltage loop is too slow to prevent the overshoot.

Solution

The simple circuitry in Fig. 6 can be used to remove the overshoot and speed up the power supply start-up characteristics. This was implemented by removing R3 and C4 and connecting the additional circuitry. Please refer to Figs. 1 and 6 for proper circuit implementation.

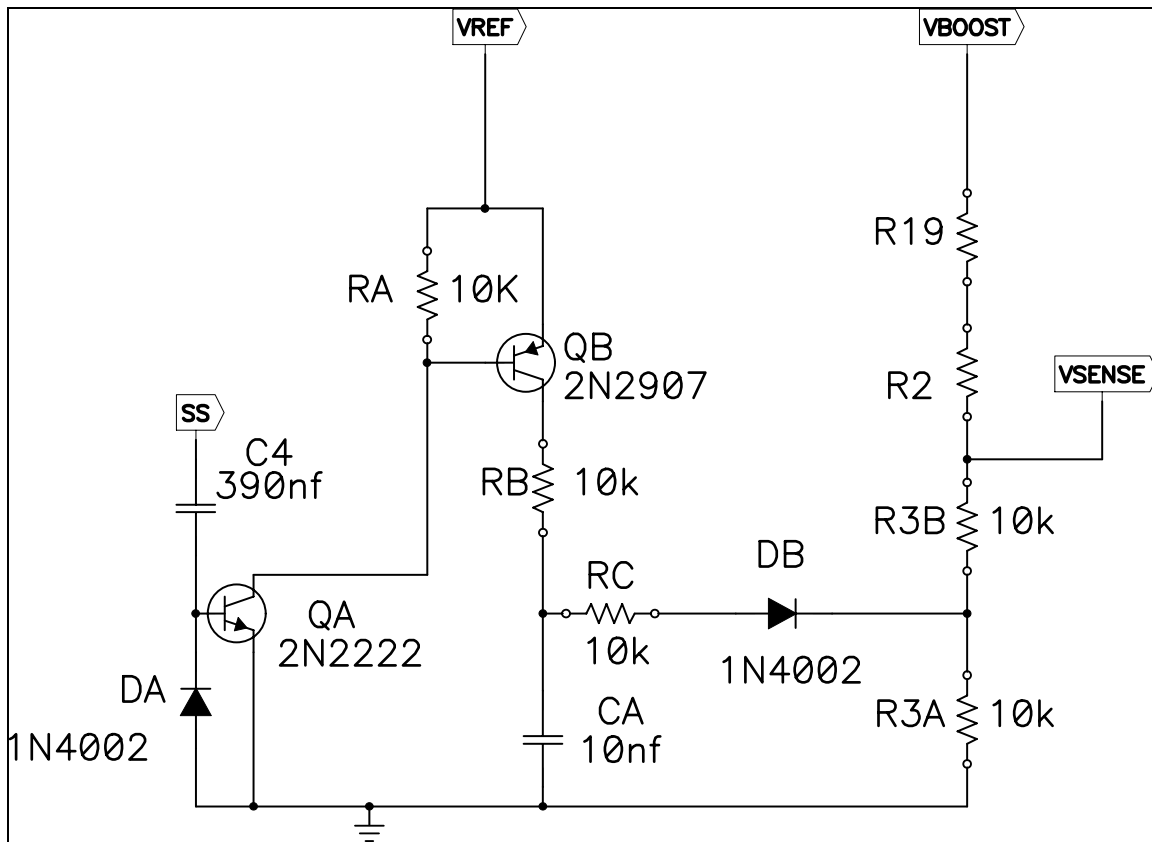


Fig. 6: Overshoot Suppression Circuitry

Theory of Operation

The voltage loop will regulate the VSENSE pin to roughly 7.5 V. The function of the circuitry is to apply 2 V to the VSENSE pin fooling the voltage amplifier during power-up. This action will cause the gate drive of Q1 to turn off when the boost voltage achieves 75% of its regulated output voltage, reducing the amount of peak overshoot seen at the output during power-up.

This circuit takes advantage of the soft-start function that is present in a lot of PWM control integrated circuits. The soft-start (SS) pin of the PWM controller provides 10 μ A of charge current until the SS pin achieves a 5-V dc level and then terminates the charge current. Diode DA, Transistors QA, QB and capacitor C4 form the timing of the circuit. While capacitor C4 is charging, transistor QA turns on pulling down on the gate of the pnp transistor QB. This in turn applies roughly 2 V to the VSENSE pin during power up through the voltage divider formed by RB, RC and R3A and diode DB. After capacitor CA is fully charged, transistor QA turns off disabling the circuit.

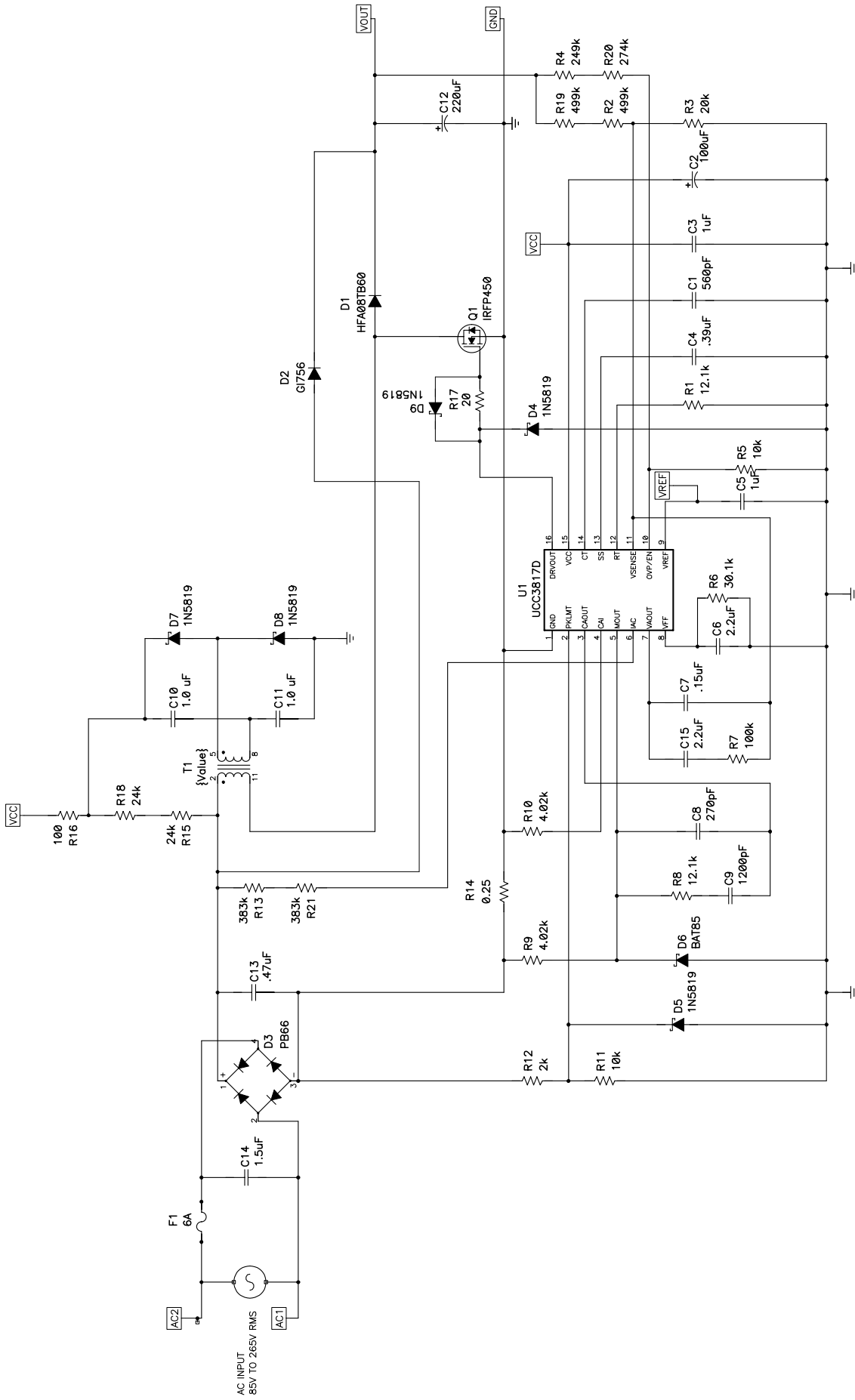


Fig. 1: Typical PFC Application

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