

# Simple Circuitry Gets That Old PFC Controller Working In A Boost-Follower PFC Application

by Michael O'Loughlin

Applications Engineering, Texas Instruments Limited, Manchester, NH

## Typical Two-Stage Off-Line PFC

Typically PFC off-line power converter systems are designed into two cascaded power stages. The first stage is a boost-converter because that topology has continuous input current that can be shaped through the use of a multiplier, and average current mode control to achieve near unity power factor (PF). However, the boost-converter requires a greater output voltage than the input and requires a second converter to step this voltage down to a usable level (see Fig. 1).

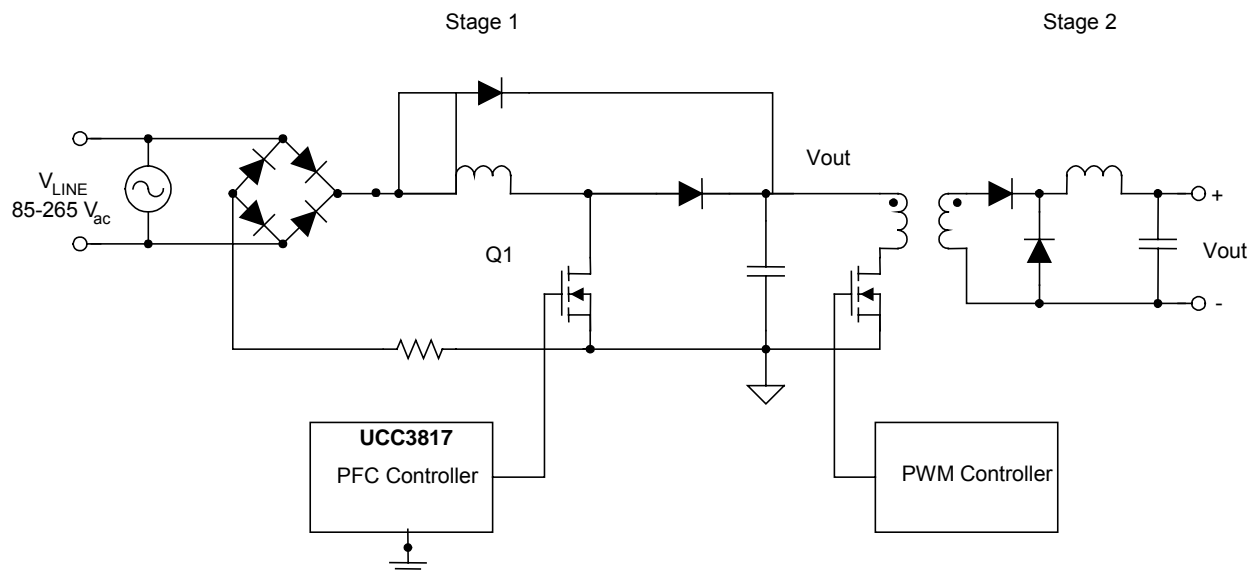
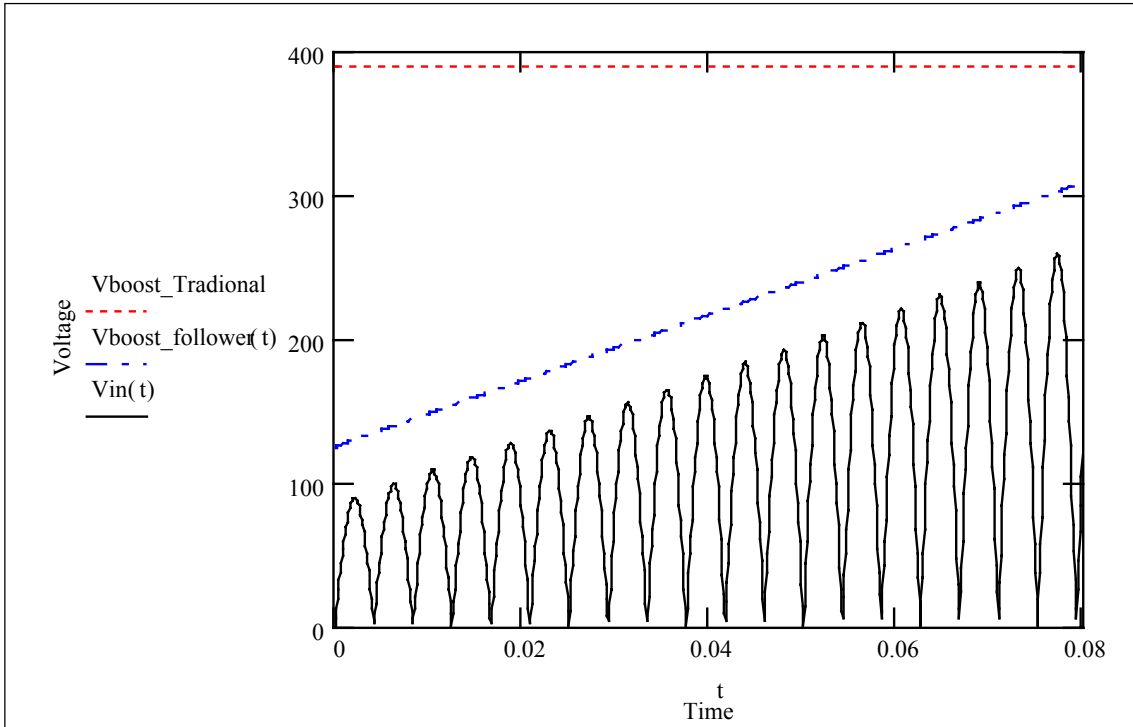


Fig. 1: Typical Two-Stage Off-Line Power Converter

## Benefits Of A Boost Follower

The boost-converter is traditionally designed to have a fixed output voltage greater than the maximum peak line voltage. However, the boost voltage does not have to be well regulated or fixed because the step-down converter can be designed to handle the variations in voltage. As long as the boost voltage is above the peak input voltage, the converter will regulate properly. There are actually some benefits in varying the boost voltage with variations in peak line voltage (i.e. boost follower preregulator). One is a reduced boost inductor size and the other is a lower switch loss at low line operation. Fig. 2 shows how a boost follower and a traditional PFC preregulator's output voltages respond with changes in input voltage [ $V_{in}(t)$ ].



**Fig. 2: Variations Of Traditional Boost And Boost Follower With Input Voltage**

### ***Reduced Boost Inductor (L)***

The boost inductor is selected based on the maximum-allowed ripple current ( $\Delta I$ ) at maximum duty cycle ( $D$ ) at the peak minimum line voltage [ $V_{in(min)}$ ] and minimum output voltage [ $V_{out(min)}$ ]. The following equations were used to calculate the required inductor for the boost power stage for a prototype power supply. A decrease in  $V_{out(min)}$  results in a decrease in maximum duty cycle, causing the boost inductor to decrease.

$$D = 1 - \frac{V_{in(min)} * \sqrt{2}}{V_{out(min)}}$$

$$L = \frac{V_{in(min)} * \sqrt{2} * D}{\Delta I * f_s}$$

$$\Delta I = \frac{P_{out} * \sqrt{2} * 0.2}{V_{in(min)}}$$

## Reduced Boost Switch Losses at Low Line Operation

In an off-line PFC converter, a large amount of the converter's power losses are due to switching losses across the boost switch, Q1. The following equations describe the FET transition loss (PFET\_TR) and part of the FET's parasitic capacitance loss (PCOSS). Where IRMS\_L is the rms current in the boost inductor, and Ton and Toff are the FET switch transition times, variable  $f_s$  is the power converter's switching frequency, and Coss is the parasitic FET capacitance. From these equations it can be observed that if the output voltage is reduced it will reduce the switching losses as well. The boost-follower PFC converter at low line voltage has a much lower output voltage than a traditional PFC boost-converter which reduces switching losses.

$$P_{FET\_TR} = \frac{1}{2} V_{out(min)} * I_{RMS\_L} * 0.9 * (t_{on} + t_{off}) * f_s \quad P_{COSS} = \frac{1}{2} C_{OSS} V_{out(min)}^2 * f_s$$

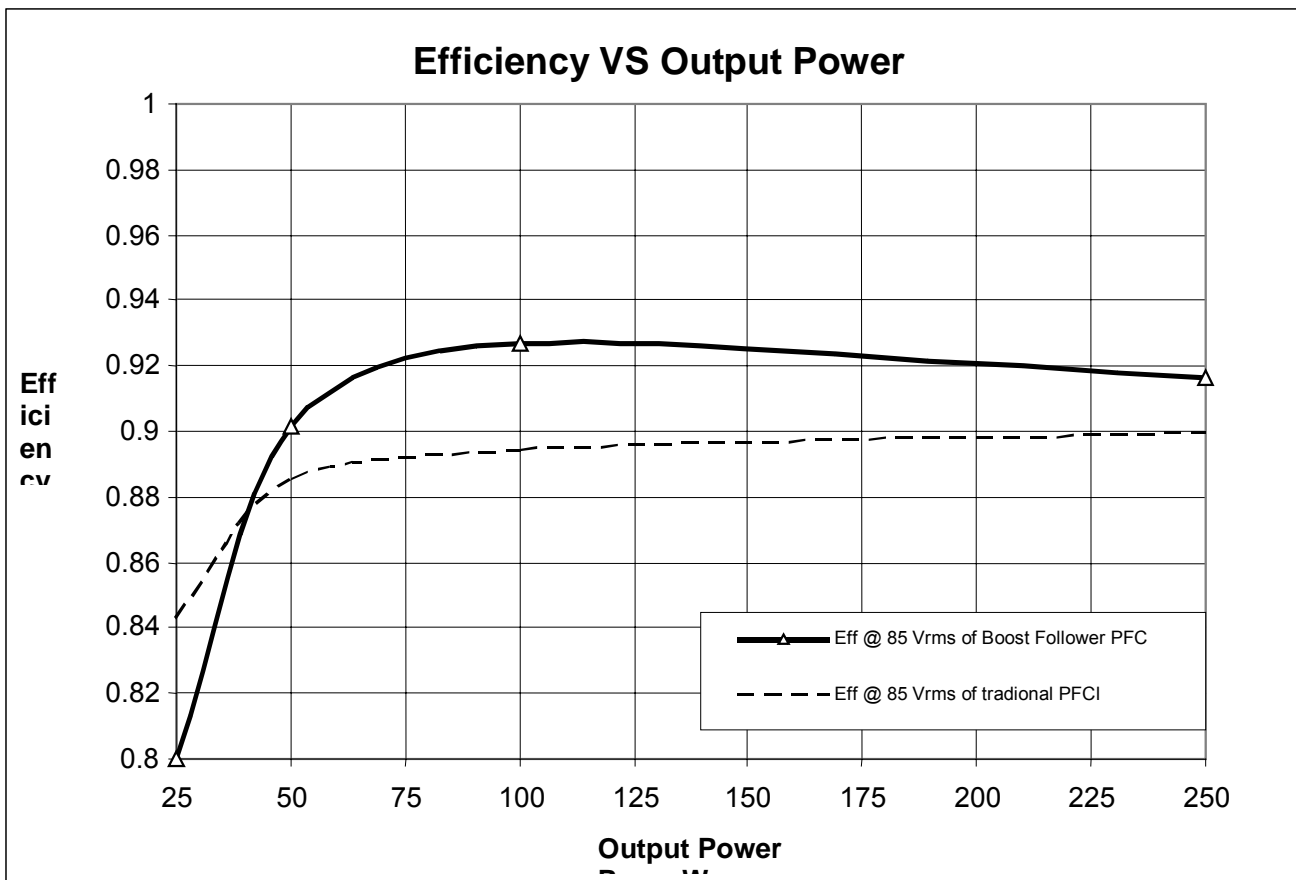
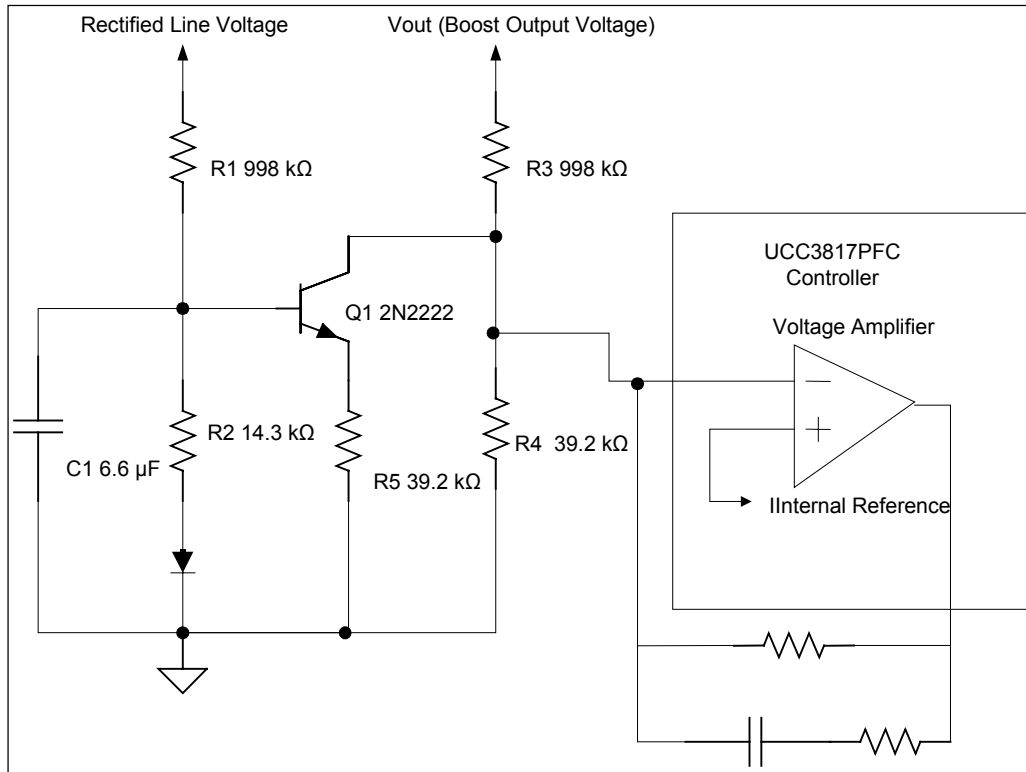


Fig. 3: Efficiencies of Traditional and Boost-Follower PFCs @ 85 Vrms

To illustrate, we built two 250 W prototype converters using a UCC3817 PFC control IC for a universal line voltage application (i.e. 85 Vac to 265 Vac). One power converter was designed with a conventional topology and 390 V output voltage. The second PFC converter was built using the boost follower technique and a varying output voltage from 230 V to 387.5 V. The boost follower was roughly two to three percent more efficient at low-line operation. Please refer to Figure 3 for the efficiency comparison.



**Fig. 4: Only 5 Additional Components Are Required For Boost-Follower Circuit**

### Additional Circuitry Needed

Designing a boost-follower PFC power stage with a typical PFC controller is not difficult and only requires five additional electronic components (see Fig. 4).

The additional components are C1, R1, R2, R3, R4, Q1 and D1, which are used to sink additional current out of the voltage amplifier's inverting signal in the voltage-loop feedback. As the rectified line voltage increases and decreases, Q1 draws a proportional amount of current through R3, causing the output voltage to change proportionately to line voltage changes. The diode is used to offset the temperature variations in Q1's base emitter junction ( $V_{be}$ ). Capacitor C1 and R2 form a low-pass filter that removes ripple voltage caused by the rectified line voltage.

## Design Example

This circuit was designed to vary the output from 230 V up to 390 V. This is roughly a 2:1 input range. The first step in designing this circuit is setting up the voltage divider formed by R3 and R4. R3 was chosen first, using the following equation to calculate the value required for R4. For this design Vref was 7.5 V and Vout(min) was 230 V.

The voltage divider formed by R1 and R2 was set up to vary the voltage at the base of Q1 from 1.4 V to 3.9 V. Care must be taken not to saturate the transistor. The following equation can be used to select R2.

$$R4 = \frac{R3 * Vref * 2}{Vout(min) - Vref}$$

Vqbl(min) is the voltage at the base of Q1 when the input voltage is minimized at 85 V rms. Vd is the forward diode drop of the circuit.

Capacitor C1 is used to filter out the rectified line voltage ripple. To limit 3<sup>rd</sup> harmonic current distortion, the filter is set up to attenuate the rectified line frequency to 1.5% of the maximum voltage at

$$R2 = \frac{R1 * (Vqbl(min) - Vd)}{Vin(min) * 0.9}$$

$$C1 = \left( \frac{R2}{R1 + R2} * \frac{Vin(max) * 0.9}{Vqbl(max) * 0.015} - 1 \right) \frac{1}{2 * \pi * (2 * f\_line) * R2}$$

the base of Q1 [Vqbl(max)]. The maximum input voltage for this design [Vin(max)] was 265 V. The line frequency (f\_line) was 60Hz.

In the final design, the output voltage increased with line voltage within 8% of where it was designed. The errors were due to the diode's forward voltage, in addition to resistor tolerances and variations in the Q1 base emitter voltage (Vbe). In this application, the boost voltage does not need a tight tolerance because the downstream converter will correct any variations in the PFC preregulator's output voltage.

## References

Lloyd Dixon, "High Power Factor Switching Preregulator Design Optimization, " Unitrode Power Supply Design Seminar SEM-700, Topic 7, 1990

Michael O'Loughlin, "UCC3819 250W Power Factor Corrected (PFC) Boost Follower Preregulator Design, " [www.ti.com](http://www.ti.com) 2002, pp 1 - 12

"POWER CONVERSION," September 1992 Proceedings, p 67

"Practical Considerations in Current Mode Power Supplies," Unitrode Applications Note SLUA110, Power Supply Control Products (PS) 2000 Data Book, pp 3 - 559

"UCC3817 Data Sheet", [www.ti.com](http://www.ti.com), SLUS395E, April 2001, p 8

## About The Author

Mike O'Loughlin is an Applications Engineer with Texas Instruments, High Performance Analog Division, in Manchester, NH. He has worked with TI/Unitrode integrated circuits for the past 11 years after earning a BSEE from the University of Massachusetts.

as published in...

analog **ZONE**

---