

Bit-Error Rate (BER) For High-Speed Serial Data Communication

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Today's serial data communication data rates continue to increase, due to bandwidth-hungry applications that include video transport, data over IP, wireless basestation, and medical applications. While data rates are driven upwards, latency requirements are still tight, specifically for full-duplex communication that involves streaming data like voice. Lower latency means less room for error correction, which in turn puts more stringent requirements on the number of acceptable bit errors in serial transmission. For example, the upcoming wireless basestation networking standard, *Open Base Station Architecture Initiative* (OBSAI), requires a BER of better than 10^{-15} .

The SerDes device is a key component in a serial communication system. The serializer block of a SerDes device accepts parallel data and multiplexes them to a single serial output. The deserializer block of a SerDes device has a clock and data recovery PLL that extracts the clock from the serial data and retimes the serial data with respect to the extracted clock. The recovered data is deserialized to provide parallel data output. As will be explained later, the intrinsic BER of a well-designed SerDes is zero. In other words, when a serializer output is directly connected to a deserializer input, and all datasheet parameters are met, there should be no erroneous data reception. In practical applications the bit errors in data communication links are caused predominantly by multiple extrinsic factors.

Applications that have very stringent BER requirements raise several key challenges:

1. Being able to be as precise as possible in determining the BER of the transmission link
2. Due to the low frequency of errors, the amount of time it will take to gather enough data to accurately measure the BER is monumental. Hence, wise estimation and extrapolation techniques need to be used to make a precise estimation of the BER in a short duration
3. Selecting the physical layer components that have jitter characteristics that will guarantee the desired BER from a jitter standpoint

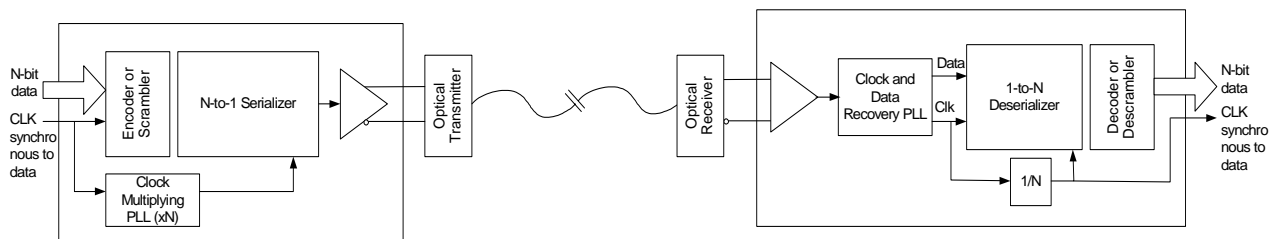


Fig. 1: Block Diagram Of Serial Digital Communications System

Sources Of Bit Errors In A Digital Serial Communications System

Bit errors can be caused in serial communications systems due to improper design or due to random events. Under these circumstances the BER is determined by the circuit design and by probability.

Bit errors can be caused in digital serial communications systems due to intrinsic or extrinsic factors.

Intrinsic errors are those errors due to the design, components and implementation of a link. These errors can be caused by internal noise sources (eg thermal noise), poor electrical connections, and (with some systems) receiver sampling errors. In optical links the errors occur primarily because of the physical components used to make the link (optical driver, optical receiver, connectors, optical fiber, etc). Errors are also caused by optical attenuation and optical dispersion. One of the largest causes of random or noise-induced errors is the optical receiver. Here light received from the fiber is converted to an electrical signal through a transimpedance amplifier (TIA). This amplifier must respond to current changes in the PIN photo detector of less than a few μA of current to detect the presence or absence of light. This low signal level makes the receiver preamplifier susceptible to thermal and shot noise, and converts these into random jitter. The serial transmitter (eg Cypress HOTLink family of transceivers) is generally never considered to be a source of errors in the link. This is due primarily to the pseudo-synchronous nature of its design. In the case of the Cypress family the transmitter operates fully synchronous to its internally-synthesized bit-clock. So long as the clock, incoming data, and power, meet their specified parameters the part should not generate any errors. The serial receiver is also generally never considered to be source of error as long as it is provided with valid power and data (meeting its data sheet requirements). The receiver present in the Cypress family is based on a high-reliability fully-differential analog PLL designed to remove all intrinsic error sources from the receiver, and to block many of the extrinsic error sources. The high jitter tolerance and high input sensitivity allows it to deal with attenuation and jitter introduced by extrinsic and intrinsic error sources. As with any electronic component, it may be susceptible to single-event-upset phenomena caused by disturbance at the atomic level; however, none have ever been observed.

The extrinsic sources of errors are caused by external sources and outside influences. These include power supply noise/ripple; electrostatic discharge; electromagnetic interference; cable/connector vibrations.

A popular misconception is that the reason for the detected errors in a communications link is the jitter accumulation in the link. While jitter definitely does play a part in determining the BER for a system, it alone does not cause errors. Jitter becomes a dominant factor in affecting BER only if all the other intrinsic and extrinsic error sources remain controlled. A link measuring minimal jitter (<0.1 UI) could become unusable if presented with a strong enough noise source.

Reference 1 provides a good discussion on understanding the sources of bit errors for both electrical and optical links.

When contribution from other sources is minimal the jitter generated by the transmitter and jitter accumulated across various points in the transmission system all the way from the transmitter to the point at which the data is recovered by the receiver affects BER. This article covers how the jitter budget of the transmission system affects operating BER and how a designer can determine if the serial link will meet the desired BER, assuming that the cause of errors is jitter present in data at the receive node of the link.

Measurement of BER: Slam Dunk Approach

The definition of BER is the ratio of number of erroneous bits detected to the number of transmitted bits:

$$\text{BER} = \text{number of erroneous bits} \div \text{number of transmitted bits}$$

Since BER depends on probability this number represents the actual BER of the link only if the number of transmitted bits tends to infinity.

If the link is set-up to transmit and receive a known data pattern it is very easy to measure the number of errors detected over the test duration by just using a simple error detector that compares the transmitted and received data. For example, if one error was observed after transmitting 10^{12} bits, is it safe to assume that the BER of the link is $1/10^{12}$? No. Due to the random nature of errors, there is no guarantee that there will be less than or equal to 1 error in the next 10^{12} bits. What if there were 3 observed errors in the next 10^{12} bits? Is it safe to assume that the BER of the link is $4/20^{12}$. The answer is no, again.

The theoretical way to obtain the accurate BER using this method is to transmit an infinite number of bits -- a practical impossibility. The confidence level of the BER number obtained increases with the measurement time. The only way to make a practical measurement using this method is to run the test for a long duration to guarantee BER with a certain confidence level.

For a standard like Gigabit Ethernet (Data rate = 1.25 Gbit/s), that specifies a bit error rate of less than $1/10^{12}$ it takes around 13 mins to transmit 10^{12} bits. In one day the number of bits transmitted would be close to 100 times 10^{12} . The BER calculated after this will give a reasonable amount of confidence on the measurement made. On the other hand the OBSAI RP3 requires a BER of less than $1/10^{15}$. Here, the time required to transmit 10^{15} bits at a data rate of 1.536 Gbit/s is around 7.5 days. The time required to make a measurement with the same amount of confidence as the Gigabit Ethernet case is much greater.

Reference 2 outlines the methodology and calculation to determine the test time for measuring BER for a given confidence level.

Jitter Measurement And BER

From a jitter standpoint bit errors are caused when the jitter present at the receiver input data exceeds the receiver's guaranteed jitter tolerance. Hence, if the absolute jitter tolerance of the receiver is known and there is a way to guarantee (by design or test) that the total jitter at the receiver input is less than or equal to the jitter tolerance of the receiver at the given BER, then BER for the link can be guaranteed.

The total jitter present at the receiver input is the sum of multiple random (Gaussian) sources of jitter and deterministic sources of jitter. Random jitter is generated due to random noise sources present in the components that are used to build the link (such as thermal noise). Random Jitter is an undesirable and unpredictable misplacement of any particular transition from its ideal position that cannot be correlated to either data-stream content, or parameters of the hardware.

Deterministic jitter refers to jitter that is bounded and arises due to deterministic characteristics of the link or the data. Deterministic jitter is an undesirable and often difficult-to-predict misplacement of any particular transition from its ideal position that can be correlated to the content of the data stream or some characteristic of the circuit or hardware. Reference 3 provides a very good discussion of sources of jitter in a digital serial communications system.

Deterministic jitter is bounded jitter and does not build up with time. Random jitter, on the other hand, is unbounded and the peak-to-peak jitter keeps growing with time, tending to infinity. Since the peak-peak jitter keeps growing with time accurately measuring it will take time equal to infinity -- in theory.

However, for truly Gaussian distributions it is possible to predict the peak-peak jitter at a given BER from the rms jitter value obtained from the distribution based on probability. This is valuable since the rms jitter value usually converges to a stable value in very short time, resulting in a quick measurement. Reference 4 offers a good explanation on the calculations needed to perform this conversion. In the presence of deterministic jitter, the deterministic edge displacement also has a random component embedded on the top of it. The total jitter (TJ) is a sum of the peak-to-peak random jitter and deterministic jitter:

$$TJ = RJ_{p-p} + DJ$$

The value of RJ_{p-p} depends on the BER and measured random rms jitter:

$$RJ_{p-p} = N * RJ_{rms}$$

The value of N for different BERs is given in the table below.

BER	N
10^{-3}	6.18
10^{-4}	7.438
10^{-5}	8.53
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069
10^{-13}	14.698
10^{-14}	15.301
10^{-15}	15.883
10^{-16}	16.444

In order to measure TJ using the above method random jitter present in the signal must be separated from the deterministic jitter. Reference 5 documents multiple methods to measure the total jitter by measuring the random jitter and deterministic jitter components (Example: TailFit, BERT Scan, Bathtub curves, Real Time Sampling, Equivalent time sampling, etc). The TJ measured at the receiver inputs at the given BER must be less than the jitter tolerance of the receiver. If there are no other extrinsic sources of errors and jitter is the only source of error that condition guarantees the BER. The jitter tolerance of the receiver is usually specified in the datasheet of the receiver device.

While measuring jitter at a particular BER the methodology used to measure the jitter must only measure the portion of the jitter that matters. By design clock and data recovery PLLs are designed to track jitter within its loop bandwidth. Usually (for well designed clock and data recovery PLLs), only the jitter outside the loop bandwidth of the CDR PLL affects BER. The measurement methodology for measuring jitter must compare the jitter present in the data to the clock -- that will have the same jitter characteristics of the clock that would be recovered by the receiver from the same data. Reference 6 offers explanation on this topic.

Well-designed transceivers will ensure the least amount of jitter generated at the serial transmitter outputs and also ensure that the maximum amount of jitter can be tolerated at the serial receivers. For example, Cypress transceivers are designed to meet jitter tolerance requirements for a wide range of standards that include Gigabit Ethernet, ESCON, Fibre Channel (1.0625 Gbit/s), OBSAI-RP3 and CPRITM.

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