

## **Distributing Network Synchronization In ATCA Systems: Part 2**

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In this second in a two-part series on ATCA systems we look at the fundamentals of the synchronization clock interface of the ATCA standard. The first part of the series is available at [http://www.analogzone.com/iot\\_0725.pdf](http://www.analogzone.com/iot_0725.pdf)

The Advanced Telecommunications Computing Architecture (ATCA), as defined in the PICMG 3.0 specification, is gaining wide acceptance as a platform for next-generation communications networks. ATCA is a highly adaptable, modular and open architecture standard that reduces the development time and cost of high-performance, high-density systems by allowing the use of standard hardware and software components from multiple vendors.

This TechNote addresses the fundamentals of the synchronization clock interface of the ATCA standard (Section 6.7 of PICMG 3.0), and discusses some of the major obstacles to overcome in order to properly distribute network synchronization in an ATCA system.

### **Synchronization Clock Interface**

ATCA forms its synchronization clock interface architecture using a set of six differential clock busses on the Zone 2 connector of the ATCA backplane. These busses are divided into three groups of two differential pairs (CLK1A/B, CLK2A/B, CLK3A/B), and are used by the system to exchange redundant network synchronization information to multiple boards in the shelf. Depending on its individual needs and functions within the system, a board may interface to any, all, or none of the available synchronization busses.

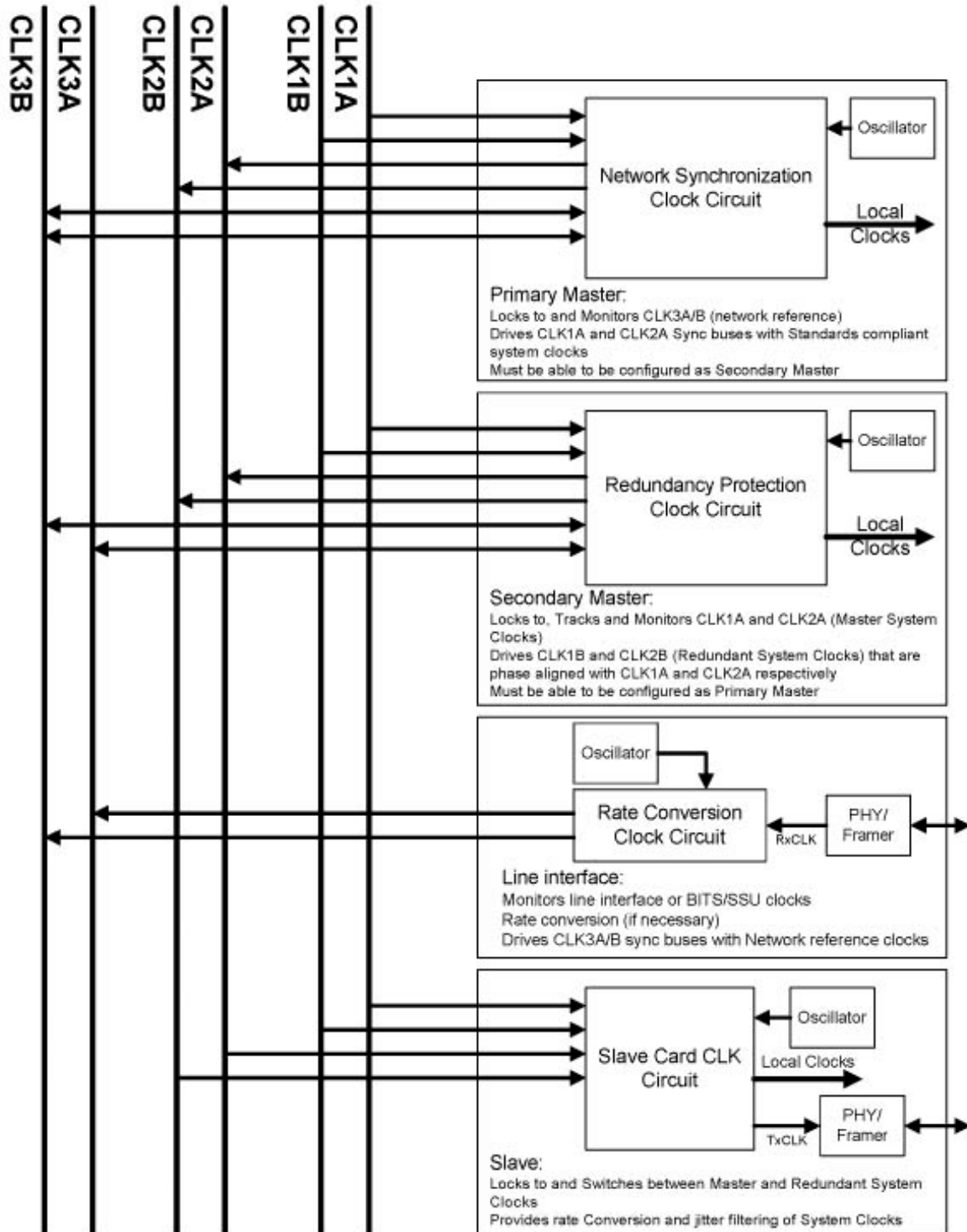
Boards that interface to the busses should support the following requirements:

- Hot-swap;
- Maintain synchronization integrity during short duration glitches;
- Present a high impedance to the bus, unless authorized by the shelf manager to drive the bus;
- At least one bus out of a redundant pair group must remain active and uninterrupted during a single board failure; and
- Provide and/or accept MLVDS differential clock pairs to/from the backplane.

### **CLK1 Busses**

The CLK1A and CLK1B busses carry a pair of redundant 8 kHz system clocks/frame pulses. Signals on the CLK1 busses must comply with Telecordia's requirements for a Stratum 4E clock as presented in the GR-1244-CORE standard. Some of these requirements include a  $\pm 32$  ppm free-run accuracy, limited wander generation and transfer, and controlled phase transients during synchronization rearrangements. The Stratum 4E requirement is a minimum requirement. Clocks

that conform to the stricter Stratum3/3E (Telecordia GR-1244-CORE) or SDH Equipment Clock standards (ITU-T G.813 option 1 or 2) can also be used on the CLK1 buses.



**Fig. 1: A-B Skew Requirements**

CLK1 frame pulse must have a minimum pulse width (high or low) of 122 ns, which is equal to the period of a 8.192 MHz clock. The rising edges of the A and B clocks must be phase-aligned within the ATCA skew requirements. The ATCA skew requirements were modelled after the H.110 bus specification, and allow a nominal 10 ns skew on the backplane between CLK1A and CLK1B. To account for PLL phase corrections, additional allowances are made to bring the maximum skew in any clock cycle to 30 ns.

### CLK2 Busses

The second ATCA clock synchronization bus is dedicated to a redundant pair of 19.44 MHz system clocks that are commonly used for SONET/SDH networks.

The 19.44 Mhz MLVDS clocks on CLK2A and CLK2B should have a duty-cycle of 50% ±10%. The skew requirements for CLK2A and CLK2B are identical to the CLK1 requirements shown in Fig. 1.

The CLK2A/B clocks are required to meet the Stratum 3/3E or SDH equipment clock (option 1 or 2) criteria outlined in the Telecordia GR-1244-CORE and ITU-T G.813 standards. Table 1 briefly summarizes these requirements.

Standard	Free-Run Accuracy	Holdover Stability (initial 24 hours)	Filtering	Output Phase Transients
Stratum 4E	+/-32 ppm	Not Applicable	Not applicable	MTIE <1.0 usec
Stratum 3	+/-4.6 ppm	<255slips (+/-3.7x10 <sup>-7</sup> )	3 Hz	MTIE <1.0 usec
Stratum 3E	+/-4.6 ppm	1.2 x 10 <sup>-8</sup>	0.001 Hz	MTIE <150 nsec
G.813 option 1	+/-4.6 ppm	2 x 10 <sup>-6</sup>	>1 Hz and <10 Hz	MTIE <1.0 usec
G.813 option 2	+/-20 ppm	4.6 x 10 <sup>-6</sup>	0.1 Hz	MTIE <1.0 usec

**Table 1: Stratum 3/3E And SDH Output Clock Requirements**

### CLK3 Busses

CLK3A and CLK3B are user-defined busses that enable centralized master system clock sources to receive external network reference clocks from a slave board located in the ATCA shelf. The CLK3A/B busses can be either a user-defined clock of frequency <100 MHz, or a derived network reference of frequency 8 kHz, 1.544 MHz, 2.048 MHz or 19.44 MHz. Network reference clocks will have a minimum high pulse width of 45 ns.

## **Architecture**

ATCA was designed to support two basic architectures: a centralized system clock source synchronization model, and a distributed synchronization system model.

### **Centralized System Clock Architecture**

The centralized system clock architecture employs a pair of dedicated master timing cards to deploy the redundant system clocks to the rest of the system. These master timing cards are equipped to receive external network references from any of the other boards in the system via the CLK3A and CLK3B sync busses or from their own external network reference interface. The timing cards synchronize to the appropriate network reference (as selected by the shelf manager) and distribute the system clocks via the CLK1 and/or CLK 2 busses for use by the slave cards located in the shelf. Which of the A or B busses are chosen as primary or secondary is arbitrary and will change during normal operation.

### **Redundancy Protection**

To ensure at least one set of valid system clocks is available to all the slave boards, the ATCA architecture provides redundancy protection. The A and B busses should be driven from separate boards to ensure robust redundancy protection. System clock failures can be detected in two ways. Hard failures of the active system clock should be detected independently by each slave card. Soft failures or out-of-range failures should be detected by the master clock sources.

If the slave card detects a failure (the absence of their primary/active reference) it must seamlessly and automatically switch to the secondary clock source. If the primary clock source is deemed out-of-specification by the redundant or secondary master card, then a procedure must be initiated to convert the secondary master timing card to the primary master timing card and stop the current out-of-specification primary clock from driving the sync bus. This then forces the slave cards to stop using an invalid clock source for their synchronization.

To convert a secondary master timing card to a primary master timing card, the following steps should be taken:

- The secondary card should be placed in holdover immediately upon detection of a failure on the primary clock. Since the secondary clock is locked to the primary clock source, this ensures at least one set of the system clocks being driven onto the sync busses remains valid;
- The PLL on the secondary card should be switched from a high-bandwidth mode, which was necessary to track the movements of the primary clock and maintain the skew requirements between the A-B busses, to a low bandwidth mode that can provide the necessary standards compliant filtering. (see Table 1);
- The secondary PLL switches its active reference from the primary system clocks (the CLK1 or CLK2 busses) to a valid network reference from the CLK3 bus; and

- The secondary card is taken out of holdover and now assumes the responsibility of the primary master timing card. This procedure should take place without causing problems on the slave cards due to transients caused by mode and reference switching.

### Timing Solutions For Centralized ATCA Architecture

Individual boards in the central architecture can be configured to provide any, all or none of the three main timing functions, as illustrated in Figure 2.

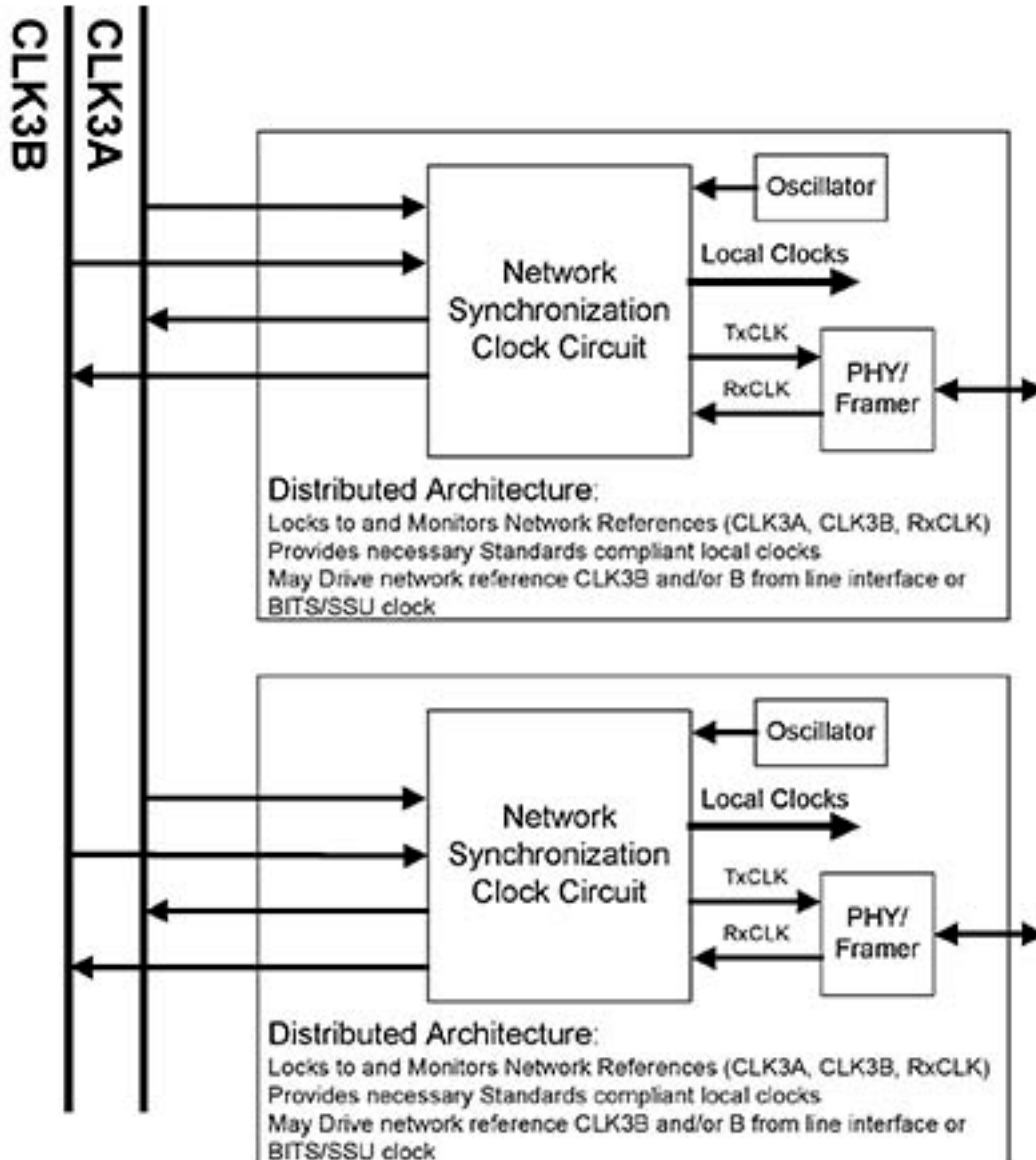


Fig. 2: Centralized System Clock Architecture Timing Functions

## **Master Timing Card Function**

The primary master card locks to one of the external network references (as selected by the shelf manager based on quality and availability) received from the CLK3A and CLK3B synchronization busses, and then provides standards compliant system clocks onto the active system clock busses (CLK1A/B, and/or CLK2A/B). The secondary master card locks to one of the primary system clocks from the active system clock bus, and provides clocks to the redundant system clock busses that are frequency and phase aligned.

The design of a master timing solution for ATCA is complicated by the fact that it must be able to perform as both primary and secondary masters. When configured as a primary master it may have to meet the strict Telecordia GR-1244-CORE Stratum 3 standards for network synchronization. When configured as a secondary master it must continuously track the reference and maintain acceptable phase alignment in the presence of jitter and wander.

The master timing solution must be able to lock to and monitor the incoming network references on the CLK3 busses and perform hitless reference switches between them in the case of a detected failure. It must provide standard compliant jitter and wander filtering, which in the case of the Stratum 3 CLK2 busses requires a PLL bandwidth of 3 Hz or less.

A precision oscillator is required to provide long-term holdover stability. The use of a compensated oscillator, such as a TCXO (temperature-compensated crystal oscillator) or preferably an OCXO (oven-controlled crystal oscillator), is needed to meet the Telecordia Stratum 3 requirements. The system must be able to lock to the master's system clock pair from the ATCA backplane. It must also be able to monitor the backplane clock and react quickly in the event of a failure on the master clock to ensure at least one set of the system backplane clocks remain operational and undisturbed. In order to properly track the primary master the secondary master must operate in a wide-bandwidth mode to maintain an acceptable phase alignment between the backplane clocks, even in the presence of allowable levels of jitter and wander.

In simpler applications where Stratum 3 or G.813 synchronization standards are not needed, and only the CLK1 busses are used for system clock timing, the master timing card design is also simplified. The strict wander filtering characteristics and long term holdover stability requirements are not needed, allowing designers to use a less complicated timing solution and a less accurate, less stable oscillator. In these applications it may make sense to consider a distributed architecture, as the main advantage of the centralized architecture is to allow designers to implement the more costly, more complicated timing functions on only two cards in the system.

## **Line Interface Function**

Boards that have access to an external reference source, such as a BITS clock, SSU or line interface receive clocks, can be configured to distribute the network reference via the CLK3A or CLK3B busses.

The shelf manager decides which boards actively drive these busses. However, the boards that supply the external network references to the synchronization busses are responsible for monitoring its external network references and driving the bus only with a valid reference. Depending on the system's design, a rate conversion PLL may be needed on these line interface cards to produce the proper clock frequency on the CLK3 busses.

### **Slave Card Function**

These boards can lock to either of the system clock busses and provide rate conversion and jitter filtering in order to supply the necessary local clocks. In the event of a failure on the active references these cards must switch to the alternate system clock bus for synchronization. Therefore, these cards must monitor the CLK1 and CLK 2 bus clocks, automatically determine which ones are valid and lock to them. No long-term holdover is required on the slave cards since the redundancy protection of the master timing cards ensures the presence of a valid reference at all times. This allows the use of a simple, non-compensated oscillator in the slave timing solution.

### **Distributed Timing Architecture**

In a fully distributed architecture there are no system clocks provided on the CLK1 and CLK2 sync busses. Instead, any board in the system that requires network synchronization uses the network references from the CLK3 busses to generate all of their local clocks. In this model boards are frequency locked, but do not have phase synchronization. It is also possible to use a combination architecture where two boards in the system provide the system clocks on the CLK1 and CLK2 busses. In this architecture, only some of the slave cards use these references to generate their local clocks, while other boards use the external network references to generate their local clocks.

### **Timing Solutions In Distributed ATCA Systems**

As there are no master timing cards distributing system clocks that meet the appropriate network synchronization specifications, the individual boards in the system must implement a timing solution that meets its own network synchronization requirements. Because of this a system that has a greater number of boards requiring a high level of network synchronization, such as Telecordia Stratum 3, may be better suited to take advantage of the centralized architecture in order to minimize costs and complexity. However, a system that has a limited number of cards requiring any network synchronization, or a system with relaxed synchronization requirements, may find a distributed architecture to be simpler and cost-effective.

## Conclusion

PICMG 3.0 defines a very simple and flexible synchronization platform that gives designers the freedom to implement application-specific features into the timing and synchronization system, while ensuring interoperability between boards from different vendors.

## About The Author

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## Further Reading

PICMG 3.0 [http://www.picmg.org/pdf/PICMG\\_3\\_0\\_Shortform.pdf](http://www.picmg.org/pdf/PICMG_3_0_Shortform.pdf)

ATCA <http://www.picmg.org/newinitiative.stm>

ATCA FAQ <http://www.picmg.org/pdf/AdvancedTCAQA.pdf>

Transporting TDM Data In ATCA Systems-Over-Ethernet

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