

## Basics of High-Performance SerDes Design: Part II

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*Part I looked at the basics of SerDes operations, and its applications, exploring the many ways jitter is defined, and measured, in high-speed serial data circuits. Here, design techniques are introduced to adapt a basic circuit to a particular application, and we look at how different media, twisted-pair cable and PCB traces, affect a SerDes signal.*

### Fail-safe And Termination Circuitry

Serializers with LVDS output buffers require a termination resistor ( $R_T$ ) at the input of the deserializer, placed physically close and matching the impedance of the differential media as closely as possible. In multi-drop or multi-point applications it is important to realize the drop in impedance that is caused by having all deserializer input capacitances on a single node. The best way to measure this impedance is to use a time domain reflectometer (TDR) sending a small, steep-edged pulse, usually less than 50ps, and monitoring the reflection to characterize inductance and capacitance. The TDR equipment then uses these values to calculate the impedance for the media.

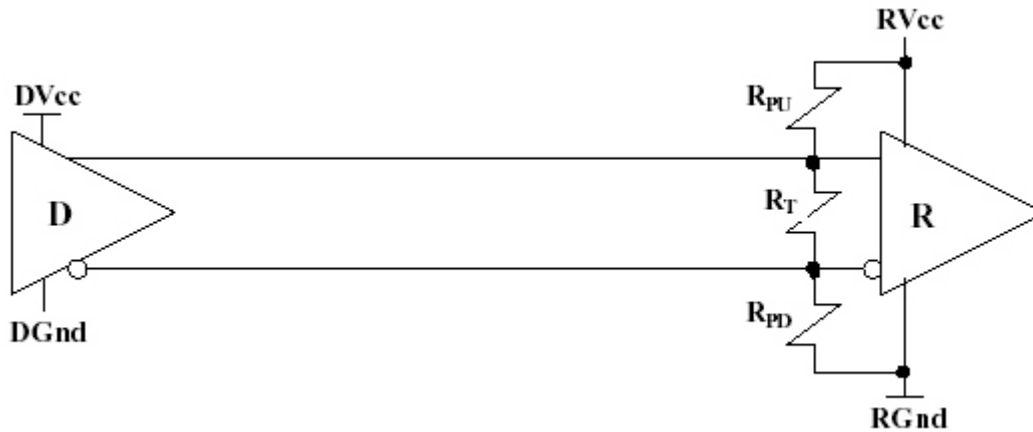


**Fig. 6: Typical LVDS Termination Technique Using Internal Failsafe**

The common approach to LVDS termination (Fig. 6) relies on the internal failsafe circuitry, describing the effect various fault conditions have on the deserializer. For example, if the application involves a cable link between the serializer and deserializer and the cable were to be disconnected from the serializer it would then act as a noise antenna. If the noise exceeds the deserializer's comparator threshold erroneous TTL data would appear on the output. Typical receiver threshold values (to cause a valid response) range from  $\pm 10$  mV to  $\pm 50$  mV.

The internal threshold could be designed to an even higher value since LVDS signals can operate as low as  $\pm 200$  mV but signals can be attenuated in some applications. Since LVDS devices enjoy broad applications a designer may plan a fully functional system switching around  $\pm 75$  mV, but the margin for noise would then be only 25 mV.

In systems where the noise level may be higher than the threshold it may be necessary to employ an external failsafe circuit, but only necessary if the noise is present when the SerDes link enters a tri-state mode and no LVDS signals are present. An external failsafe circuit is simply a light pull-up/-down on the differential pair (see Fig. 7) to overcome the noise on the line and to guarantee a known static state.



**Fig. 7: LVDS Termination Technique Using External Failsafe Circuitry**

It is important that only enough failsafe bias should be applied to overcome the noise since the circuitry will be present in normal SerDes operation and excessive current in the pull-up/-down resistors will overpower the drive of the serializer and degrade signal integrity. When sizing resistors  $R_{PU}$ ,  $R_{PD}$ , and  $R_T$ , also remember that the Thevenin equivalent of the three {parallel combination of  $R_T \parallel (R_{PU} + R_{PD})$ } must still match the effective impedance of the transmission media. The desired common mode voltage for the link - the level the LVDS signal toggles around, typically 1.2 V - must also be considered and numerous application notes from various vendors exist on this subject. After designing a failsafe circuit a breadboard test with noise added will help validation.

Some vendors use a technique known as active failsafe, a deserializer circuit to monitor the condition of the LVDS signal. If the lower threshold is exceeded on the differential signal the deserializer output switches to a known valid state and continues to monitor the circuit for a valid signal. Unlike external failsafe the active failsafe has minimal effect on the LVDS signal since it is only seen when the device enters failsafe mode. If the IC contains this type of failsafe it is not necessary to apply an external failsafe and the designer should contact the respective vendor to verify if this applies.

## Lock Time

In SerDes 10:1 devices the serializer's SYNCH pins, when pulled high, cause the device to output a synchronization pattern that allows the deserializer to easily pick out the clock and lock the PLL: The deserializer's /LOCK pin remains high until the internal PLL locks up. Connecting the SNYCH and /LOCK pins acts as a feedback loop between the two devices with the serializer continuing to output a SYNCH pattern, a slow series of

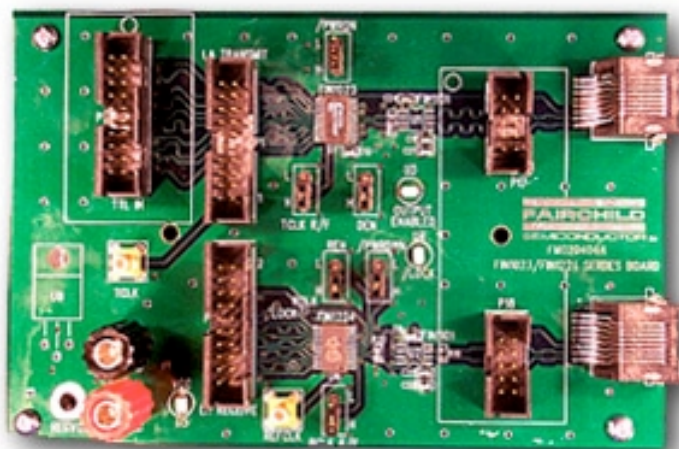
equal length lows and highs, until the deserializer acknowledges its PLL is locked. At that point the deserializer will drive the /LOCK pin low and the serializer will output the data on the TTL inputs. The time required to lock is listed in the datasheet for each vendor. Note that no inverter logic is needed for the lock feedback connection between the two devices. This type of feedback is currently only available with the 10:1 family as other SerDes devices do not have the /LOCK pin on the deserializer. The feedback system is not a requirement for 10:1 devices as the deserializer can lock to random data - but the lock time can vary, and it is recommended that the designer use the feedback loop in 10:1 SerDes applications to maintain reproducible lock times.

SerDes devices such as the 28:4 and 21:3 families, used in displays, run a separate twisted pair from the serializer clock output to the deserializer clock input making it easier for the deserializer to distinguish the clock, and so lock prior to an average vendor specification of 10 ms; during which time both the serializer and deserializer have locked to their respective clocks and correct data is transmitted.

### **Media Evaluation**

Because SerDes requires minimal wiring between the devices the technology is open to numerous cable types and what follows is a comparison of different lengths of what is commonly called CAT-5 cable. Associating a frequency with a given cable length is very beneficial when selecting an interface technology for a specific application.

The primary goal of a demo board designed by Fairchild Semiconductor's Ensigna Lab was to establish interoperability but had added features, one of which allowed the evaluation of various media with RJ-45 connectors (see Fig. 8) connected to the serializer output and deserializer input to allow easy swapping of a variety of cable lengths.



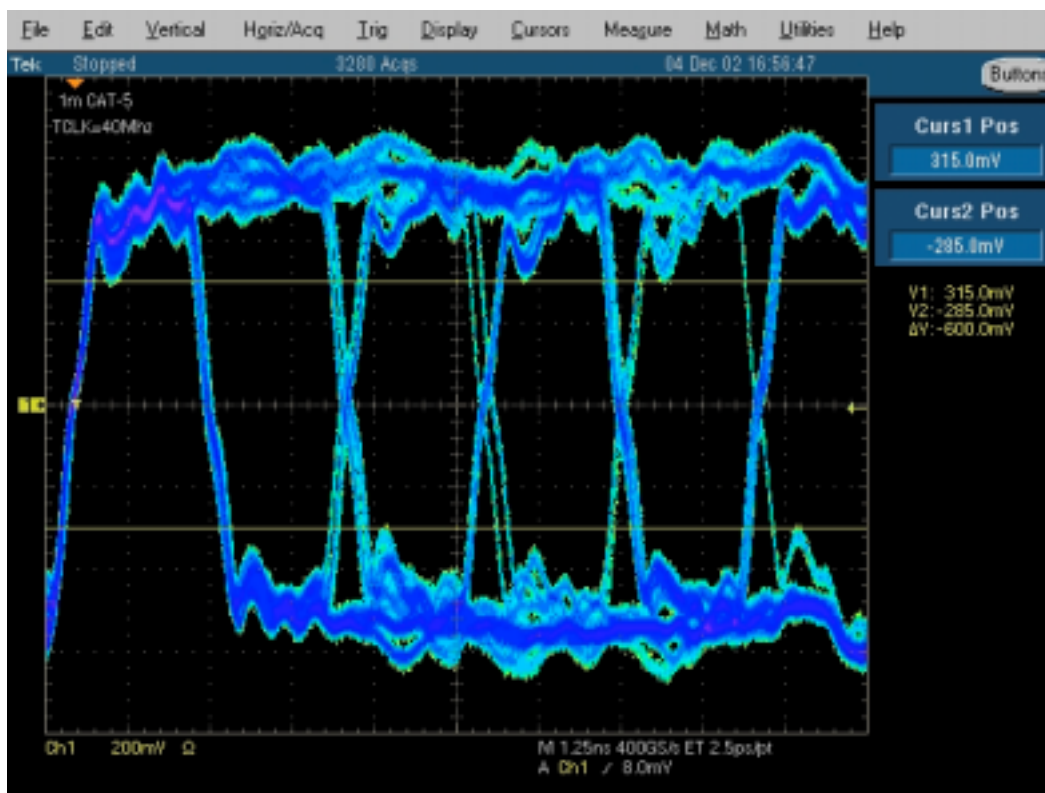
**Fig. 8: SERDES 10:1 Demo Board Used In Media Evaluation**

## CAT-5 Cable

Different lengths of CAT-5 cable were placed between the 10:1 serializer and deserializer devices. Only one of the twisted pairs was used, with an RJ-45 connector on each end. With CAT-5 density up to four 10:1 devices could transmit on a single cable and if each operated at the maximum transfer rate of 660 Mbit/s, 2.64 Gbit/s could be maintained.

The first test involved a meter length of 100- $\Omega$  unshielded twisted pair (UTP) cable (Note: shielded cable provides increased signal integrity.) A scope capture (Fig. 9) that was taken at the 100 $\Omega$  termination resistor shows the start bit beginning the sequence - always a high pulse for 10:1 devices - at the far left with the following nine bits. The low pulse preceding the start bit is actually the stop bit from the previous word. Horizontal resolution on the scope was set to show only a data bit eye diagram for the first four bits.

The purpose of this experiment was not to demonstrate the performance of the 10:1 serializer in the demo board but to observe changes in eye pattern when the cable length was changed. Scope acquisition was set to infinite persistence to show jitter and in all plots a differential probe was used actually measuring the absolute differential between the two traces, regardless of polarity: So the waveform amplitudes are read as double.

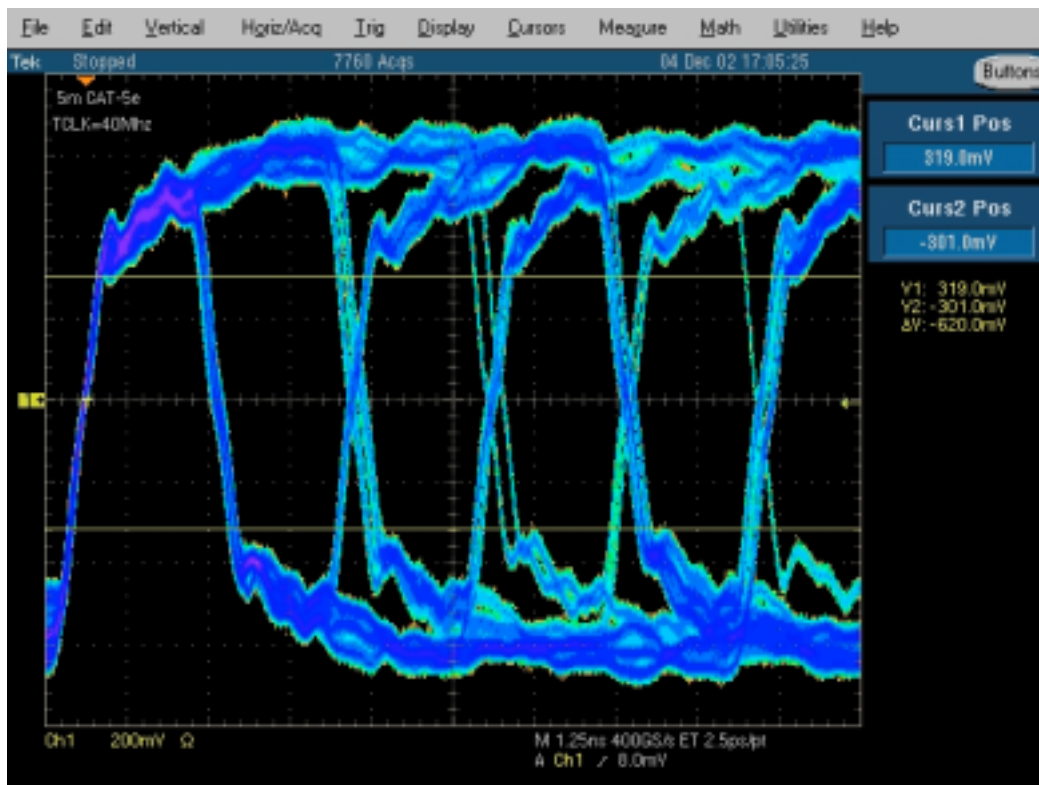


**Fig. 9: Serial Signal At Deserializer Input After 1 m Of CAT-5, TCLK 40 MHz**

Fig. 10 shows the separation of the serializer and deserializer in a test using a 5 m length of CAT-5e cable, an enhanced version of standard CAT-5. Note that the eye pattern

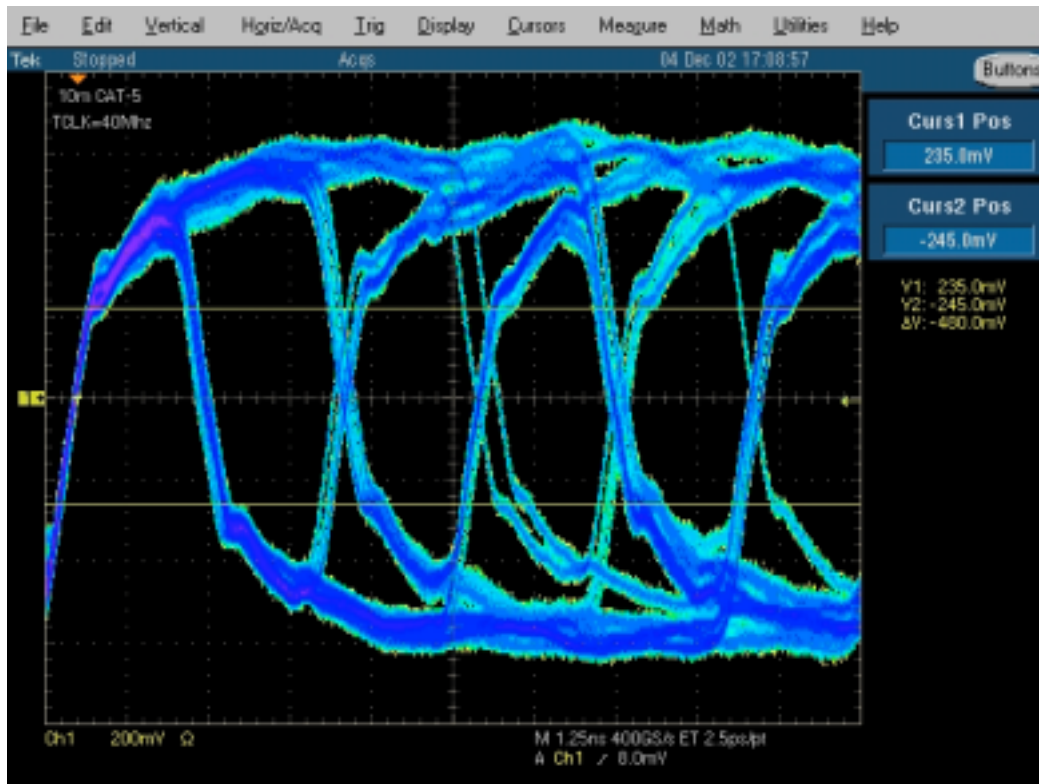
begins to close slightly due to horizontal jitter on a few edges but the overall integrity of the eye is very good. The same 40-MHz clock is sent to the TCLK input of the serializer.

It is important to point out the data-dependent jitter on some of the rising/ falling edges: The TTL data sent to the serializer is not a simple, repeating one/zero combination, rather it is “random” in nature. Ten vectors containing a wide variety of one and zero combinations were generated and repeated so data-dependent jitter exists in the plots, evidenced by two distinct falling edges on bit one. A device employing 8B/10B encoding would minimize this type of jitter.



**Fig. 10: Serial Signal At Deserializer Input After 5 m Of CAT-5e, TCLK 40 MHz**

Last, a 10-m length of CAT-5 was used to link the serializer and deserializer using the same clock frequency as the previous plots. As Fig. 11 shows the eye amplitudes begin to close, but even more prominent is the increased data-dependent jitter. At this frequency the resulting jitter is minimal compared to the overall eye width, or unit interval (UI.) If the TTL clock input frequency were to be increased to 66 MHz this 300 ps of data-dependent jitter could become an issue. Because of the accurate strobe positioning of the 1:10 deserializer, a fair amount of random and deterministic jitter is allowed, but refer to the vendor’s datasheet for specific values.



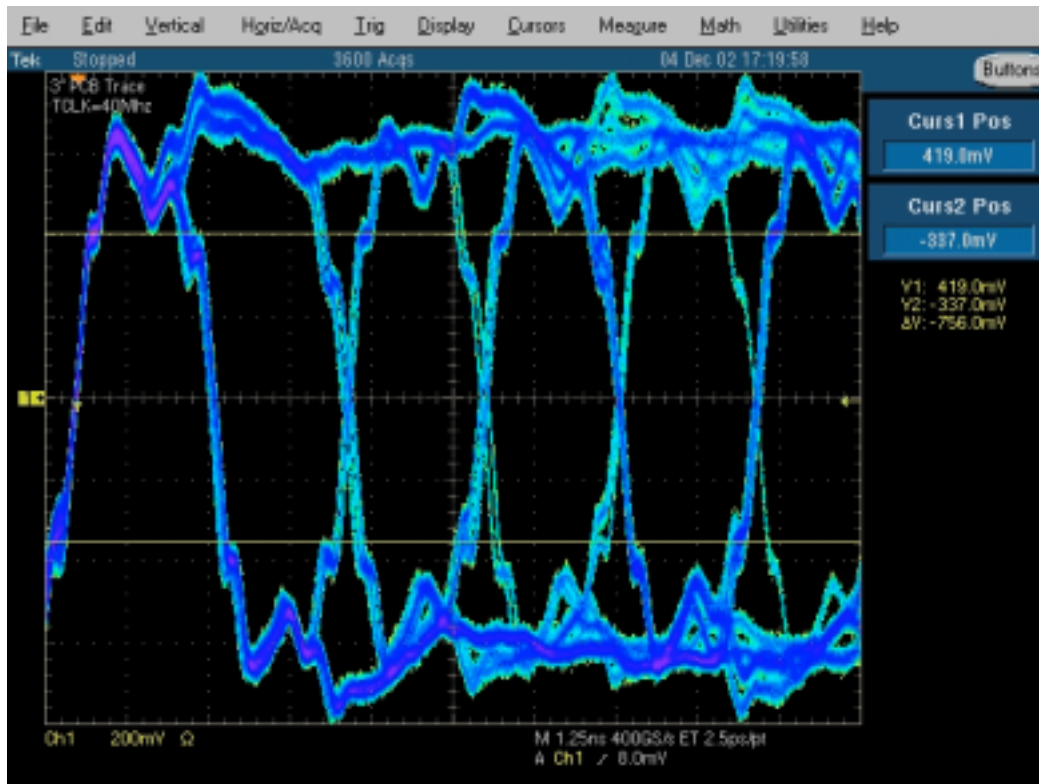
**Fig. 11: Serial Signal At Deserializer Input After 10 m of CAT-5, TCLK 40 MHz**

In any design the only way to know if the eye pattern is large enough for the strobe positioning for the deserializer is to use a Bit Error Rate Test (BERT.) When comparing two vendors' ICs it is important to use the same data pattern, perhaps a standard K28.5 pattern.

### Printed Circuit Board

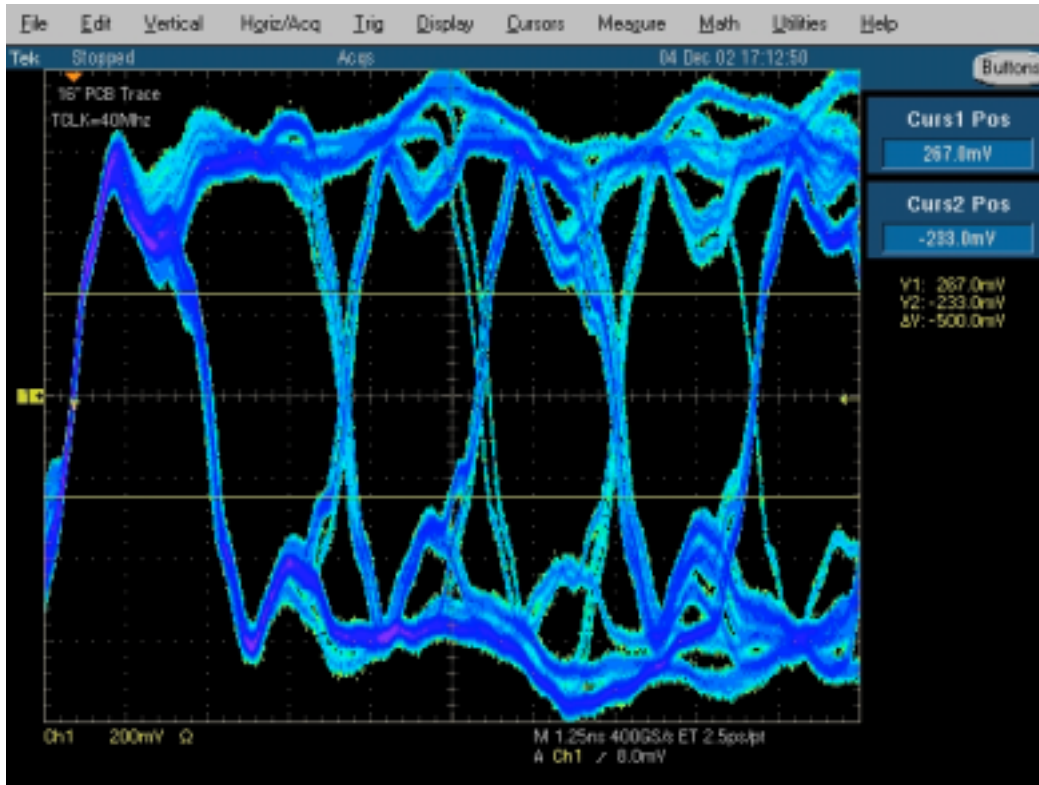
As always PCBs can be used as a sole transmission media, as would be the case in a backplane or multi-drop environment. During the cable tests the serial signal traveled through about 1.5 inches of PCB prior to reaching the RJ-45 connector and then traveling through the cable media. For PCB tests a pseudo point-to-point backplane was added to the demo board consisting of a 100 mil connector at each end with two serpentine traces with electrical lengths of 3 and 16 inches. The lengths were selected by wire links and with no cable in the RJ-45 connectors the serial signal passed along the PCB backplane.

The 3 inch evaluation is shown in Fig. 12. Impedance mismatches are easily observed - note the sharp spikes in the upper and lower LVDS limits. Jitter is minimal compared to even the shortest length of cable tested. Shortening stub lengths and using a quality differential connector with impedance matching throughout would increase signal integrity. Again, the purpose of this plot is not to show the performance of the devices but to allow the designer to compare different trace lengths in a controlled environment.



**Fig. 12: Serial Signal At Deserializer Input After 3 inches PCB With Connectors**

The board was then modified to channel the serial signal through a 16 inch PCB trace with all other conditions remaining unchanged (see Fig. 13.) Edges roll over more sharply at the upper and lower corners due to the increased trace length. Still, there is ample upper and lower margin before encroaching on the estimated maximum deserializer threshold limit of 100 mV.



**Fig. 13: Serial Signal At Deserializer Input After 16 inches PCB With Connectors**

### SerDes Summary

The general advantages of SerDes are well established with the major one being dense throughput with minimal traces between the serializer and deserializer. The high frequency of the data bits in this serialized path partners well with LVDS technology, capable of noise rejection and minimal power consumption.

As shown, SerDes devices can drive both cable and PCB over various lengths. Keeping in mind some of the general topics mentioned here a designer can easily convert an existing TTL application to a high-speed SerDes system. Application details such as impedance matching, matched line lengths, and jitter sources play a key role in the success of the design. The designer must note these items and follow the vendor's guidelines in the datasheet to assure tolerances are met. After a designer has climbed the SerDes learning curve expanded throughput applications become even easier to achieve.

### Future Roadmap

Although SERDES has been around for a while it is still considered an emerging technology in many regards. With some vendors already releasing full-duplex devices designers can expect to see even greater throughput and much larger packages in BGAs.

As redundancy becomes increasingly popular newer SerDes releases - like Fairchild's FIN7216 Quad 8-bit device - will offer completely redundant data communication with unlimited timing control. Expect to see more encoding schemes adopted and more elastic buffer implementation. Regardless of device features, understanding datasheet specifications and applying that performance to the design at hand will always be required.

### **About the Author**

Ed Suckow, applications engineer for SerDes products at Fairchild Semiconductor, is responsible for research and definition for SerDes and LVDS technology. He formerly worked in GTLP applications with Fairchild Semiconductor, in power supply design with NASA, and on project management for the US Army.

For more information on SerDes design:

<http://www.fairchildsemi.com/products/interface/index.html?aprilad>

