

Superior Card-Edge Protection Using Discrete I/O Driver Devices

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What are the specific tradeoffs that the designer and/or product manager should consider when developing product requirement specifications? This article reviews the potential effects of classical ESD for semiconductors and discusses the tradeoffs of using certain solutions, with an eye to which applications may or may not be adversely affected by this integration.

As ASIC (application-specific integrated circuit) and FPGA (field programmable gate array) speeds increase while die geometries decrease, discrete logic and I/O interface devices are becoming increasingly important for protecting these high-performance devices from Electrostatic Discharge (ESD) type events that occur in real-world applications. Events such as voltage spikes and high inrush currents can wreak havoc on state-of-the-art devices. However, discrete interface and logic devices employing robust I/O structures and sophisticated ESD schemes can mitigate these potentially damaging events with great effectiveness.

As the world changes to faster, more portable technology, electronic products continuously evolve to meet improved performance standards and more demanding application requirements. This often means faster data rates, increased functionality, and lower manufacturing costs, while still adhering to a lightweight form factor. This also means electronic building blocks (ICs) can be redesigned into single devices, like ASICs or FPGAs, to meet these requirements. This consolidation, however, comes with certain hidden tradeoffs that, unfortunately, may not even be recognized until final product testing or even until the product is deployed in the field.

Application Environment

Devices such as simple calculators and portable radios have very limited electrical interfaces to the outside world and thus have limited ESD exposure with the human interface being plastic knobs/buttons that have little path to an IC chip's innermost nodes.

In contrast, cell phones now can have USB ports, high-speed data, antennae and power ports. Automotive applications may pass high-speed data to remote sensors for control of key systems such as windshield wipers, lights, or steering and brake controls. Industrial controllers may interface to remote functions through CAT-5 cable, flex circuitry or simply a PCB in order to pass key information at high speed. It is these types of more complex systems that can be subject to ESD events through normal maintenance and servicing, or a simple environmental change. All of these types of interfaces can have direct access to ESD-sensitive high-speed nodes that may be easily damaged.

What is ESD?

A natural, everyday occurrence, Electrostatic Discharge is the transfer of charge between dissimilar, unequally charged materials. An ESD event can be both intentional and unintentional. Aircraft employ static discharge wicks to continuously provide a discharge path so that an accumulating charge does not disrupt sensitive communication and navigation equipment. However, it's usually not the intent after walking across a room to shake hands with a co-worker, and with the extension of your hand, receive a shock strong enough to send you backwards. Similarly, this same ESD event can permanently destroy an electronic device such as a phone under the right circumstances.

How Do ESD structures differ from FPGAs and ASICs to discrete devices?

FPGAs and ASICs are increasingly designed to incorporate as many functions, functional standards and I/O options as possible into the very smallest packages. This integration results in often using 0.18- or 0.13- μm technology for low-voltage operation and low-power consumption.

Discrete I/O devices often use 0.35- μm technology or larger, and can easily accommodate both the LVDS (low voltage differential signaling) driver and ESD structures. Discrete I/O devices easily lend themselves to the high current and voltage requirements necessary to thwart ESD events of many amperes and kilovolts, and can deliver excellent signal integrity right to the card edge. Table 1 shows a comparison of currently-available FPGA and ASIC devices for the I/O pins.

Device	Technology	Rated ESD I/O Pins	I/O Speed Per Port
Typical Discrete I/O Device	0.35 μm	HBM >10 kV	Approx. 600 Mbyte/s
Typical FPGA	0.13 μm	HBM 1.0-2.0 kV Maximum	Approx. 800 Mbyte/s
Typical ASIC	0.18 μm	HBM 2.5 kV Maximum	Approx. 600 Mbyte/s

Table 1: ESD Comparisons Between FPGA, ASICs And Discrete I/O

What harmless activities can invoke ESD events with today's electronic devices?

Many maintenance, configuration and movement activities can invoke ESD events if not properly managed, including:

- Inserting a line card with I/O pins exposed (card into your PC)
- Connecting a cable to a printer, laptop or digital camera
- Connecting a replacement sensor module to an automobile electrical system
- Placing a cell phone on top of a car dashboard, that then slides as the vehicle moves

The impact of an ESD event on semiconductor devices can be virtually a non-issue, or it can be catastrophic. Which category a semiconductor device falls into depends on the circuit design, semiconductor ESD structure design and, finally, the application that the semiconductor is exposed to. ESD has traditionally affected semiconductors in three ways:

- Immediate and catastrophic failure
- Degraded performance
- Latent failure

Circuit Design Strategy For ESD

Many large ASICs and FPGAs contain ESD protection circuits that are intended to be effective primarily during manufacturing. Typically, the ESD voltage rating for these ASICs and FPGAs is in the 1000 - 2000V range. This rating is because incorporating large structures onto a high density ASIC or FPGA can drastically increase both size and cost.

While 1000 - 2000V ESD protection may be adequate during controlled manufacturing, it is no match for a typical ESD event that can occur on I/O pins in a typical application. Outside of a manufacturing environment, ESD events affecting I/O connections can easily reach 10 kV. Sometimes, a discrete ESD protection array can be incorporated. This is an array of protection diodes that are used with the I/O pins, and can work well assuming the data rates are slow enough to not disrupt signal integrity. This, in effect, limits the maximum data rate that can be achieved when incorporating ESD protection arrays.

Semiconductor Design For ESD

Most semiconductors incorporate structures to protect pins from accidental ESD events. These structures are especially important on I/O pins where an ESD event is most likely to occur.

Application Design For ESD

Fortunately for most semiconductors the incidence and likelihood of an ESD event is reduced once they have been installed into a PCB and into an application. This reduced incidence is because all pins of a semiconductor are soldered or socketed to some node on a PCB and are connected to low-impedance traces or cables that are common to power or ground. In the event a pin is connected to a high-impedance path such as a control or data, this element often has some limited ESD protection. Additionally, this connection is through a PCB trace that has an intrinsic capacitance that can attenuate an ESD event.

However, as mentioned previously, in today's highly mobile society I/O pins can be subjected to the hostile ESD environment known as the outside world. This encounter can be as simple as replacing a line card for maintenance, connecting a remote sensor circuit to its controller, or simply connecting an interface cable to a cell phone! In each case, while most semiconductor pins are connected as designed, the interface I/O pins connected to the outside world can be subjected to large ESD events, fatal to the semiconductor, and unknown to the user.

Diode Arrays Of I/O Pins

Zener diode arrays can be a good choice to protect I/O pins if data rates are relatively low and when controlled impedance paths are not necessary. Unfortunately, zener diode arrays can introduce significant capacitance and must be located in close proximity to the incoming point of the ESD event. For many applications, such as cell phones and DVD read/writers and other electronic devices, the data rates can be 500 Mbyte/s or more. Here, signal integrity can degrade and the Bit Error Rate (BER) can increase. LVDS type signals can have rise and fall times <1.0 ns, and in order to achieve good signal integrity at high data rates, usually a 50Ω impedance must be maintained. (100Ω for LVDS drivers.)

Impact Of Zener Diode Array Capacitance

A review of a typical zener diode array will identify the input capacitance characteristic. These datasheets will often show that the capacitance that is inversely proportional to the reverse voltage can be greater than 20 - 35 pF when a relatively low reverse voltage in the 350 mV range, typically found with LVDS, exists. Unfortunately, 27 pF at 500 Mbyte/s data rates can have an impedance of around 30Ω , and less with faster edge rates!

The following oscilloscope photos were taken to illustrate the effect of capacitance on rise time, using a typical LVDS driver at 500 Mbyte/s; with a standard 100Ω termination load placed approximately 20 cm. from the driver through a cable to represent an actual jittery application. The measurement was taken at the 100Ω termination, while the capacitance was added at the driver card edge. For purposes of clarity, only one side of the differential signal was displayed. Fig. 1 is without the effect of zener diode capacitance, while Fig. 2 has the zener diode 27pF capacitance.

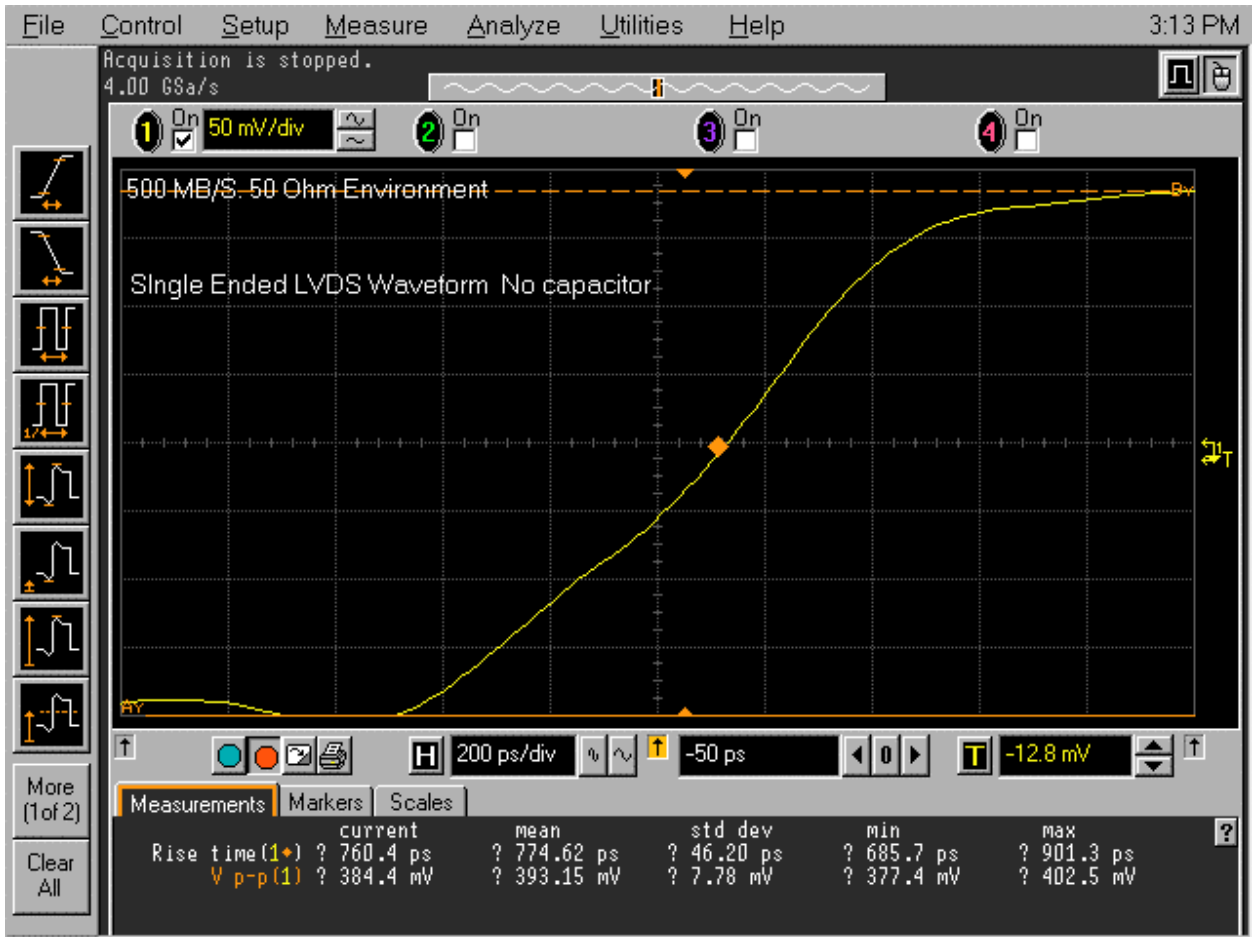


Fig. 1: 500 Mbyte/s With No Zener Diode Array Capacitance

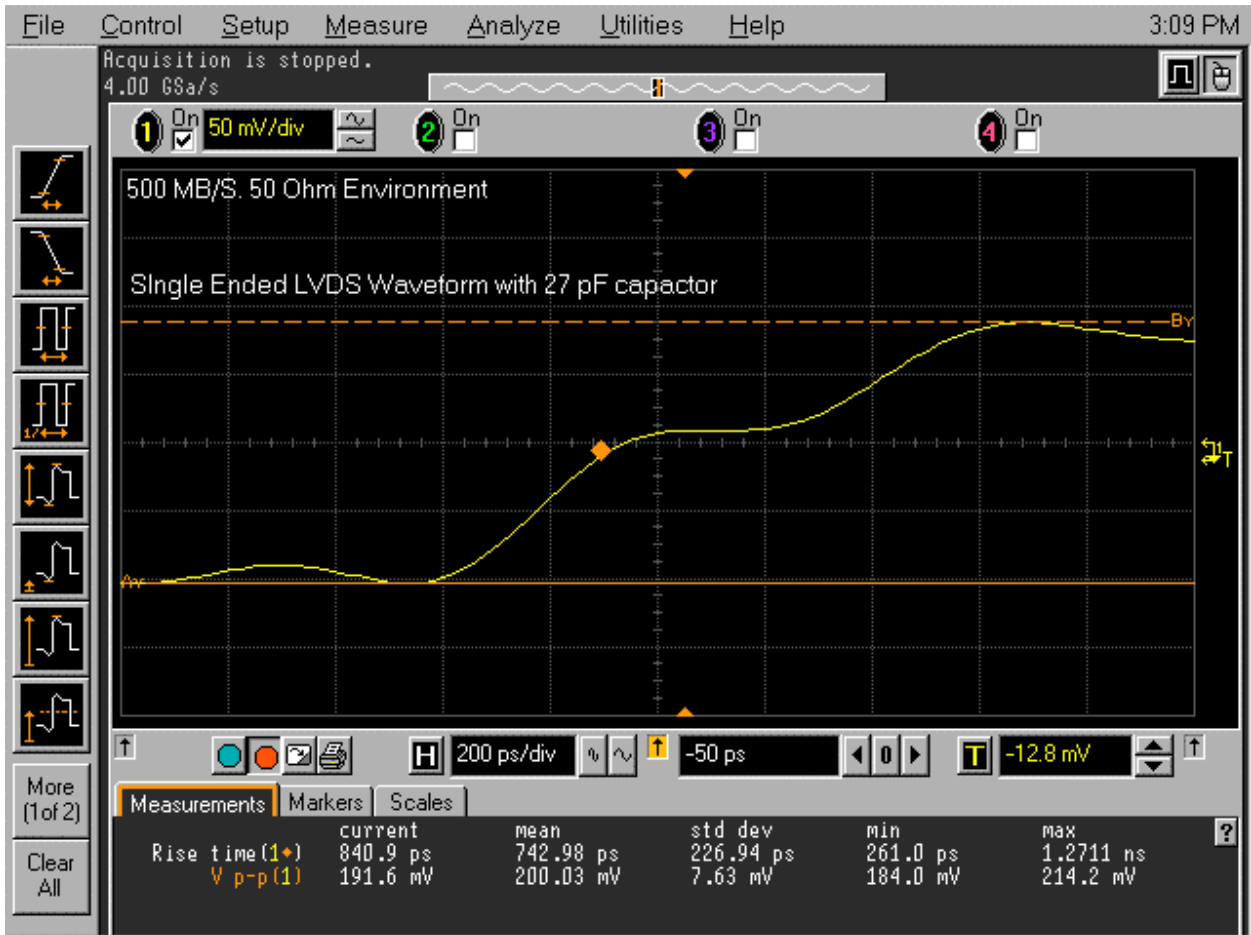


Fig. 2: 500 Mbyte/s With Zener Diode Array Capacitance

Analysis

LVDS (Low Voltage Differential Signaling), according to the TIA/EIA-644 standard, is nominally 350 mV, with a range from 250 mV to 450 mV. Additionally, the 20 - 80% rise time (and fall time too) is usually <1.0 ns, with a standard deviation of about 46 ps.

Fig. 1. No zener diode array capacitance:

- With this configuration, both the rise time and magnitude remain well behaved and within specification

Fig. 2. With zener diode array capacitance:

- With this configuration, the magnitude is attenuated such that the LVDS signal is outside of specification. The rise time remains within specification, however the waveform has become distorted with a reflection. In addition, the standard deviation has increased from 46 ns to 226 ns!

Layout Requirements Of ASICs And FPGAs

Often ASICs and FPGAs are high pin count devices that are physically very large. A review of a commonly known FPGA shows that this can be up to 1020 pins in a 33 mm by 33 mm package. With FPGAs this size, it's a challenge to correctly route the many control, signals and clock lines while trying to maintain signal integrity and a flow-through architecture. Because of this expansive routing and interconnect, large FPGAs and ASICs are located away from a card edge and often more toward the center of a PC board. This means that the FPGA or ASIC I/Os can be located a long distance from a connector or cable, and zener diode protection array. As will be discussed, this calls into question the effectiveness of the zener diode protection array.

Additionally, PCBs and cards usually require automated handling during assembly. The tooling for such assembly processes often holds the board from the edge and sides. Because of this tooling and the board support required, manufacturing losses can increase if the tooling is placed immediately adjacent to large sensitive FPGAs and ASICs.

Layout Requirements For Zener Diode Arrays

Zener diode arrays are usually placed near the point of ESD intrusion -- usually at the edge of a PC board edge or card. This keeps the currents and voltage mostly off the board and away from sensitive semiconductors. It is usually an advantage to place a significant distance between the ESD protection and ASIC or FPGA because it allows the PCB capacitance and inductance to attenuate the effects of an ESD event. Unfortunately with today's smaller electronic devices, the placement of a zener diode array can be right next to the semiconductor that it is intended to protect. Furthermore, if the zener diode array is not placed directly on top of the trace it is intending to protect, and has even the shortest traces to this node, its effectiveness can be significantly reduced due to the inductive reactance of that trace. Even a small amount of inductive reactance can limit the effect of the zener diode array, and result in a partial ESD event reaching the ASIC or FPGA.

Standards

There are three predominant standards in use today:

- Human Body Model (HBM): This is based on MIL-STD-883C method 3015.7
- Machine Model (MM): This is a Japanese based standard that uses an LCR network. C is 200 pF, R and L vary per definition
- IEC61000-4-2 is an international standard that defines the testing and measurement techniques used to evaluate ESD immunity. This is an equipment-level specification intended for use with electric and electronic equipment, which may be subject to ESD from personnel or objects near this equipment

Each of these standards enjoys widespread use and it is important, when comparing ESD voltage ratings, that the same standard is applied to each device. However, and of

particular interest recently, is the increased use of the IEC specification in addition to the HBM and MM. It is very important to recognize that the IEC specification is a system-level specification intended for equipment; however, it appears to be now used much more at the component level. Since this is an equipment specification, it is good practice to determine the test environment and equipment used when claiming compliance to this specification.

Additional Advantages Of Discrete I/O Devices

Discrete I/O devices offer the following advantages:

- ASICs and FPGAs can run cooler, as the power dissipating components (I/O drivers) can be placed elsewhere on the card or PC board edge
- Routing density can be drastically reduced using a serial stream from the ASIC and then deserialized at the card edge through discrete devices if necessary
- ASIC and FPGA throughput can be increased by using serial output and then routing that data through card-edge discrete repeaters
- Discrete I/O devices such as LVDS offer superior EMI behavior over LVTTTL type signals
- As circuit board interface standards evolve, only the interface devices require update and ASICs or FPGAs can remain the same

Summary

Using discrete I/O devices makes good sense as data rates increase, especially in environments exposed to high ESD. LVDS standards-based I/O devices are designed and characterized to provide excellent signal integrity well into 500 Mbyte/s data rates and beyond. Most I/O devices have very high pin specific ESD specifications that often far exceed those of ASICs and FPGAs. This higher specification can significantly increase the margin of circuit protection and reduce the adverse effects of ESD, such as degraded performance, latent or catastrophic failures, on the most susceptible pins.

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