Signals-From-Noise
Single-Bit ADCs in a Nutshell - Part III

by Dave Van Ess, Principal Application Engineer, Cypress Semiconductor

In our last installment http://www.analogZONE.com/iot_0205.htm we explored how to build delta-sigma modulators, handy little devices that convert an analog input into digital densities. Now we're going to put them to use as building blocks that let us construct several different kinds of ADCs that you'll find interesting, and maybe even useful for your work.

Delta Sigma Modulator (DSM)

The delta-sigma modulation converts an analog input into a digital density. It is a basic building block of mixed-signal design. It is as fundamental as the digital flip-flop is to digital design and it deserves its own symbol. A DSM symbol is shown in the figure below.

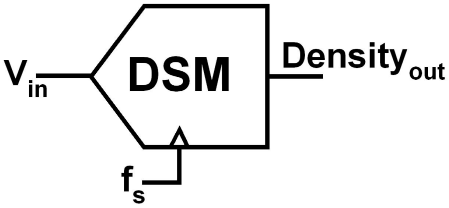

Fig. 1: New Delta-Sigma Modulator Symbol

Just as with a flip-flop it is not necessary to know how it is constructed, just that it has the defined behavior of a delta-sigma modulator.

The easiest way to measure the density is to use a counter and timer as shown below.

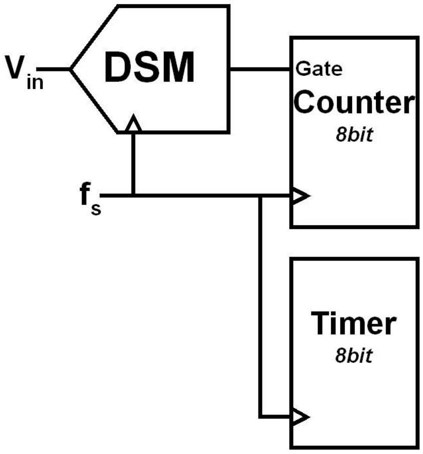

Fig. 2: Eight-Bit Incremental ADC

The counter increments each cycle that the density output is high. The timer counts the number of cycles to be processed. An eight-bit timer allows for eight bits of resolution. This topology is called an Incremental ADC.

Although an incremental ADC is easy to build, it is possible to extract more information from the DSM with the appropriate digital filtering as is shown below.

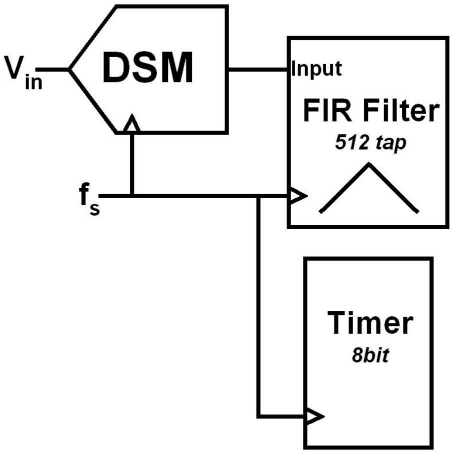

Fig. 3: Decimate By 256, 11-Bit Delta Sigma Converter

The FIR filter has 512 taps and decimates the data by 256. The result is an output with 11-bits of resolution. This topology is called a delta-sigma ADC.

A DSM has other uses than the front half on an ADC. Last month's column had a block diagram for a buck converter power supply. It relied on a triangle wave ADC in the control loop. The figure below shows the same power supply with the ADC replaced with a DSM.

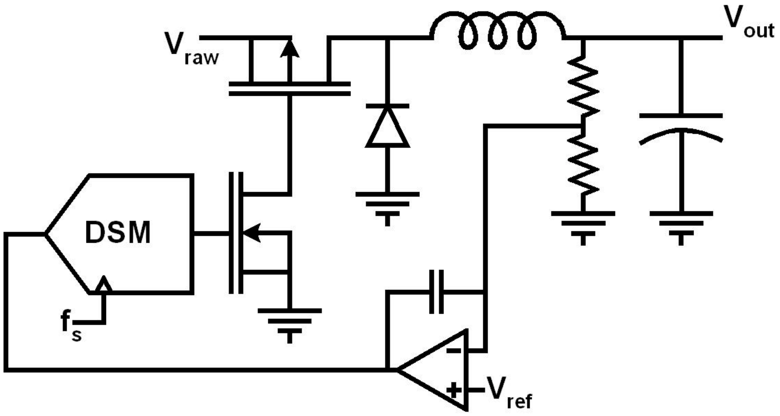

Fig. 4: DMS-Controlled Power Supply

The output is compared to some reference. If the output becomes larger than the desired value, the integrator swings in the negative direction. This voltage level is fed to the DSM where its density output decreases. With the FET now on less time, the output voltage also decreases. It works the opposite for a decreasing output voltage.

When a filter is applied to the density output of a DSM, the signal is converted back to an analog value. If the density output is optically isolated before being filtered, the result is an analog isolator as shown below.

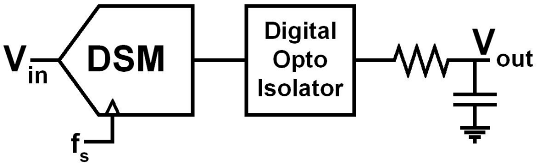

Fig. 5: Analog Isolator

The density output is a digital signal where low is defined as –Ref and high defined as +Ref. Positive times positive is positive. Negative times negative is positive. Positive times negative is negative. This single bit multiplication can be done with an exclusive NOR gate. The relationship is defined by:

$$V_A \Leftrightarrow Density_A$$

$$V_B \Leftrightarrow Density_B$$

$$V_A \cdot V_B \Leftrightarrow Density_A \overline{\oplus} Density_B$$

The block diagram below is of an analog multiplier. With the inputs tied together the output is the square of the input. It is necessary to each DSM have a different sample frequency. (If the same input signal and sample frequency are fed into identical DSMs, their outputs would always match and their XNORed result would always be high.)

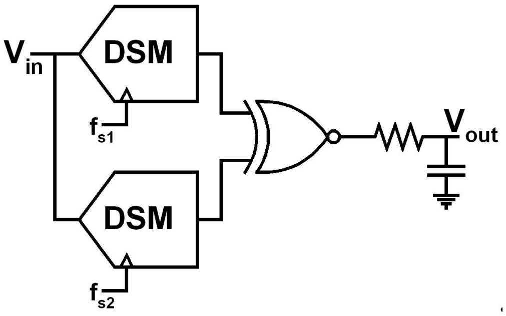

Fig. 6: Analog Multiplier Configured As A Squaring Circuit

Again I will implement this with a Cypress CY8C27443-24PXI programmable system on a chip. I use two switched capacitor blocks to construct ratiometric (AGND = ½V_{dd}, Ref = ±½V_{dd}) DSMs. One has a 1-MHz sample rate, the other 500 kHz. Their outputs are logically combined with on-chip logic resources and brought out to a pin. The low-pass filter is a built with a 16.2 kΩ resister and 0.01 µF capacitor. The plot below is of the 4 V_{pp} 100 Hz sine wave and the filters output.

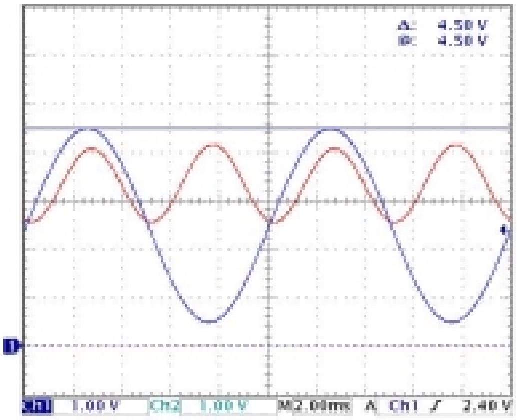

Fig. 7: Analog Multiplier Configured As A Squaring Circuit

Note that a 2 V peak signal above analog ground is 80% of the positive range. The output is 64% of the positive above analog ground or 4.1 V. A 2 V valley is 80% of the negative range. Again, the output is 64% of the positive range. When the input is at AGND, so is the output. The output frequency is also double the input frequency. This plot confirms that a squaring function was correctly implemented. This is a four-quadrant multiplier and the four-quadrant analog multiplier is the Holy Grail of analog design. Being able to construct one with a couple of DSMs and some glue logic is remarkable.

The last example used a filter to restore the density output back to an analog signal. You could just as easily have used digital hardware to measure the output density. Such an ADC would calculate the average (mean) of the input voltage squares. Using the CPU to perform a square root of the answer would result in a root-mean-squared or rms value. Ac measurements can now be easily made.

A single-bit ADC is just a method of converting an analog signal to a digital output density. When coupled with digital hardware to measure this density, the result is a value accessible by your system CPU. It can also be used outside this conventional application to inexpensively implement desirable functions.

Postscript

I have been using DSMs for seven years now and I am still finding interesting applications for them. It really is a concept every engineer needs to understand. I believe the best way to understand DSMs is to play around with them. If you spend a little time messing with the input and viewing how the output changes it will become intuitive.

To assist you with this I have built up a PSoC project with a switched-capacitor DSM and a switched-capacitor multiplying DSM circuit to fit on an eight-pin DIP part. If you already have a Cypress PSoC development system I can e-mail you the code for the project and you can program one yourself. If you don't have one handy, don't fret. I found a couple of tubes of the parts in inventory last night and programmed them. If you would like one of these chips just e-mail me your mailing address and include "Signals-From_Noise DSM Offer" and I'll send you one along with some basic instructions.

Next month I want to write about Sallen Key filters. The title will be *What Sallen Key Filter Articles Don't Tell You About Sallen Key Filters*. Till next month!

About The Author

Dave Van Ess is a Principal Application Engineer at Cypress Semiconductor. He is an electrical engineer with experience in hardware, software, and analog design. Dave joined Cypress in 2000. He has nine patents for medical systems, signal processing design, and PSoC digital block enhancements. He has written numerous User Modules, application notes, and articles. He graduated sigma cum barely with his BSEE from the University of California, Berkeley, 1977.

An engineer by training, a poet by temperament, an outlaw in Nebraska, and a heck of a nice guy, Dave has worked in many different industries. His work experience includes test and measurement equipment, measurement and control systems for high energy physics research, and underwater acoustic transmitters and receivers deployed in open sea and artic ice fields. Electrons fear him! Women revere him!

Dave can be reached at dwv@cypress.com

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