

Signals-From-Noise Single-Bit ADCs in a Nutshell - Part II

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Last month in Part 1, http://www.analogzone.com/iot_0101.htm I introduced the concept of single-bit ADCs and gave examples of a single-bit DAC generated ADC and triangle waveform single-bit ADC. I also introduced the concept of *density*, the digital stream produced by a single bit DAC that can be converted to an analog value for use as a comparison voltage within an ADC. (If you still find density little tricky to grasp, see my previous column *Single-Bit DACs in a Nutshell* http://www.analogzone.com/iot_0904.pdf for a quick refresher.)

In this column, we'll put these two concepts together and use them as building blocks for self-modulating ADC circuits.

Self-Modulation

The two previously ADC methods discussed required some hardware to generate an analog compare value. The circuits shown below are self-modulating.

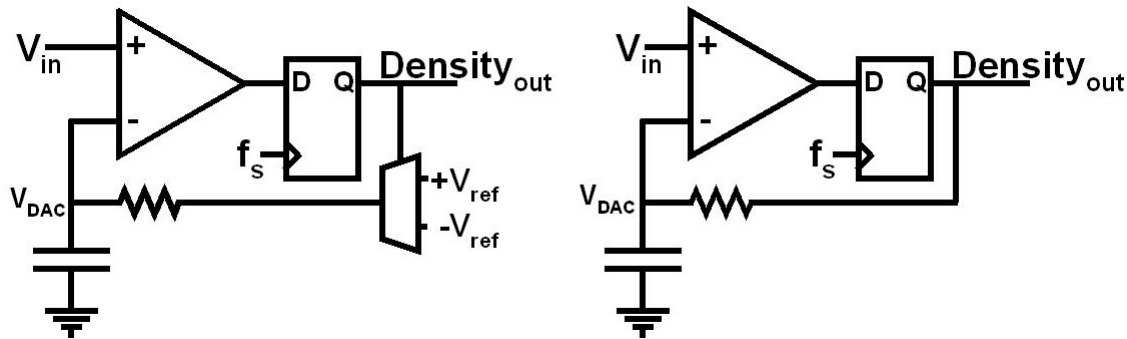


Fig. 1: Self-Modulating Single Bit ADCs (With References And Ratiometric)

The one on the right uses the supply voltage (V_{dd}) as the reference. Again, this is called ratiometric. This will be the topology discussed because it can easily be fabricated with components lying around your bench. (If you are a software guy and don't have components lying around your bench or don't even have a bench, this can easily be fabricated with components found on some hardware guy's bench. He either gets in later than you or leaves earlier than you, if you get my drift. If he complains, remind how many times you have helped him debug his god-awful code.)

If the input voltage is greater than the generated DAC voltage, then the comparator's output is high. The flip-flop samples this output and generates a logic high output that causes the capacitor to charge. This capacitor continues to be charged for as many cycles as its voltage is less than the input voltage. When its voltage becomes greater than the

input voltage, the comparator output goes low, causing the capacitor to discharge. This charging and discharging causes the DAC voltage to hover around the input voltage.

The amount of hover depends on the severity of the filtering. Given a sample frequency of 1 MHz, a supply voltage of 5 V and an input voltage of 2.5 V, the comparator toggles high then low for a 50% density value. The frequency is $1 \text{ MHz} \div 2$, or 500 kHz. For a 4 V input the comparator is high four cycles then low one cycle for an output frequency of $1 \text{ MHz} \div 5$, or 200kHz. The farther the input signal is from the middle of the range, the lower the output frequency becomes. At the limits of ground and the supply voltage, the frequency is zero. As the filter's roll-off frequency is lowered, the amount of hover is reduced, resulting in better accuracy. However, this lower frequency requires a longer time for the DAC to settle out to a large change of the input voltage. A good rule of thumb for this type of topology is to set the roll-off frequency to 1/1000 to 1/10,000 of the sample frequency. For a sample frequency of 1 MHz this works out to a filter roll off somewhere in the neighborhood of 100 Hz to 1 kHz. These low roll-off frequencies result in delays of tens of milliseconds to sudden changes of the input voltage.

A spreadsheet simulation of this circuit has been included: **SelfModulationExample.xls** http://www.analogZONE.com/iot_0205.xls Given the input voltage, supply voltage, sample frequency and roll-off frequency of the RC filter, it plots 1024 cycles of the generated DAC voltage and error term.

Digital hardware can be used to time a specific number of operation cycles and to count the number of times the comparator output was high. Given these two values it is possible to calculate the digital density. With this density value it is possible to calculate what the input value must have been.

This type of single-bit ADC is slow, but it can be built with very few components. If your microcontroller has a spare comparator, timer, and counter, it is possible to construct an ADC with just a single external RC filter.

This topology uses the average of the quantized difference as feedback. This quantized output is either **+Ref** or **-Ref** no matter how small the difference. The negative feedback attempts to make the DAC voltage match the input voltage so, by definition, their difference is small. This saddles the filter with the chore of removing a lot of harmonics.

Delta-Sigma Modulation (DSM)

Suppose instead of averaging the quantized difference, the averaged difference is quantized. The left side of the figure below shows that a low-pass filter can be built by integrating the difference of the input and the output. The left side shows the integrated difference to be quantized. (A signal is said to be quantized when it is digitized and then restored back to an analog value. Some resolution is lost.)

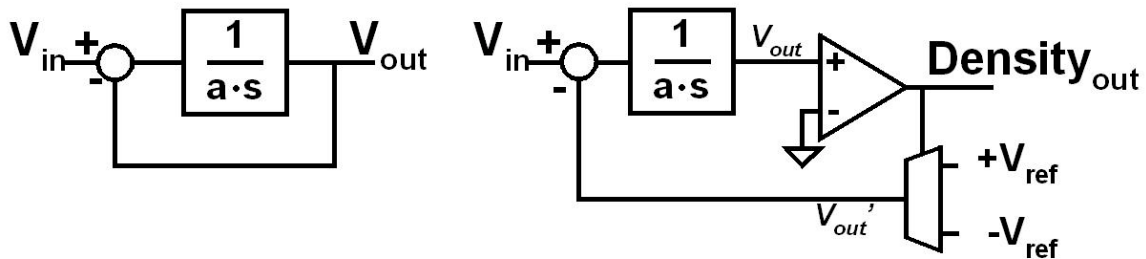


Fig. 2: Low-Pass Filter Block And Quantized Output Of The Averaged Difference

This topology is called delta-sigma (Δ - Σ). Delta is for the difference circuit. Sigma is for the integrator. Because of the feedback, the average of the input will equal the average of the quantized output. Digital hardware can be used to time a specific number of operation cycles and to count the number of times the comparator output was high. Given these two values it is possible to calculate the digital density. With this density value it is possible to calculate what the input value must have been. The figure below shows how they can be implemented with op amps.

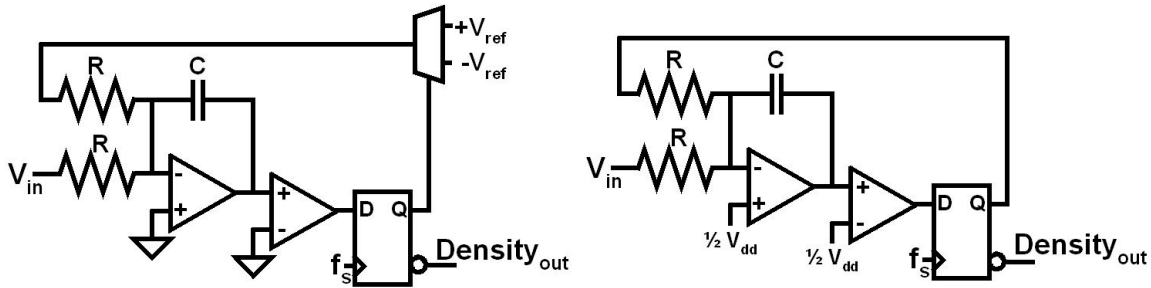


Fig. 3: Delta-Sigma Modulator (With References and Ratiometric)

Again, the ratiometric is the easier to implement with the analog ground defined as $\frac{1}{2}V_{dd}$ and reference voltages $\pm\frac{1}{2}V_{dd}$. The resistor and capacitor value must be selected to keep the integrator in range; that is, it can move no more than $\pm Ref$ in one period of the sample clock with the full range input ($\pm Ref$). The RC product is determined by the equation:

$$\frac{Ref}{f_s RC} < Ref \quad RC > \frac{1}{f_s}$$

Applying a safety factor of two, the equation becomes:

$$RC = \frac{2}{f_s}$$

Given a sample frequency of 1 MHz, the RC value is 2 μ s. One solution is to set C to 470 pF and R to 4.22 k Ω . If the sample frequency is changed to 2 MHz, then the RC value must be changed. Most likely R would be set to 2.10 k Ω .

For this example I have decided to implement a switched-capacitor delta-sigma modulator. The topology is shown in the figure below.

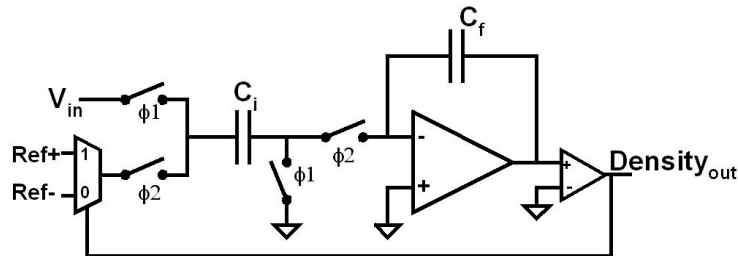


Fig. 4: Switched-Capacitor Delta-Sigma Modulator

I implemented it using a switched capacitor block in a Cypress CY8C27443-24PXI programmable system on a chip PSoC. I did so because the PSoC DSM is self-contained so it can be built with no external components.

The selection of the RC values for a standard DSM depends directly on the sample frequency. With the effective resistance of a switched-capacitor input being $1/f_s C_i$, the recommended RC value translates to the equations:

$$RC_f = \frac{2}{f_s}$$

$$R \Leftrightarrow \frac{1}{f_s C_i}$$

$$C_f = 2C_i$$

These values are independent of the sample frequency. They do not have to be changed if the sample frequency changes.

I used a switched capacitor block to construct a ratiometric ($AGND = \frac{1}{2}V_{dd}$, $Ref = \pm\frac{1}{2}V_{dd}$) delta-sigma modulator with a 1 MHz sample clock. The plot below is of a 4 Vpp, 7 kHz sine wave input and the generated density output.

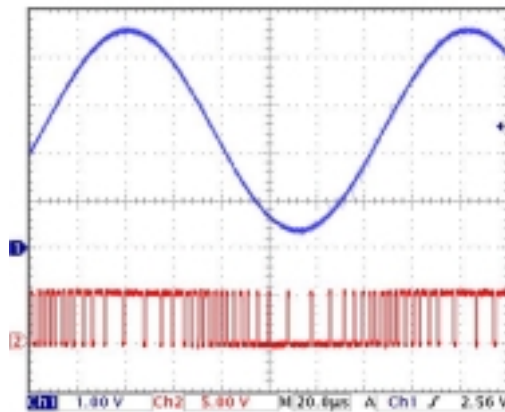


Fig. 5: Density Output For A 4 Vpp, 7 kHz Input

Note that the density is roughly 90% at the peak of the sinusoid and 10% at its lowest point.

The mind boggles at the potential applications for such a versatile little circuit! In fact, we'll devote most of the next installment of Signals-From-Noise to expanding on these concepts, and using them as building blocks for self-modulating ADC circuits.

Until then, feel free to write me with any ideas you might have at dwv@cypress.com.

Postscript

I received an e-mail from a reader. It isn't important why, but what snagged my interest was that he mentioned being a 64-year-old engineer. I have the utmost respect for any engineer that can stay technical their whole career. Tracy Kidder, author of *The Soul of a New Machine*, used the analogy that engineering is like pinball. If you play pinball very well your reward is that you get to play again. The same is true with engineering. If you do it well, your reward is that they let you do it again. You keep playing until either you do not want to, or they won't let you play anymore. You may become a spectator or you may just leave, but either way you don't play anymore. I think all any of us really ask is to leave this profession on our own terms, at the time of our choosing. My father was a NASA engineer and I can remember him working so hard to stay in the profession. At 55 he became eligible for retirement and could now leave on his own terms. When I called him to wish him a happy birthday, I could feel the load had lifted off him. He had made it. He stayed around a couple more years and then left... on his own terms. Every 10 years it's great to be an engineer. Five years later it sucks. I have been through two layoffs, countless downsizing, rightsizing, and corporate mergers but I manage to keep playing. The alternative is a real job.

About The Author

Dave Van Ess is a Principal Application Engineer at Cypress Semiconductor. He is an electrical engineer with experience in hardware, software, and analog design. Dave joined Cypress in 2000. He has nine patents for medical systems, signal processing design, and PSoC digital block enhancements. He has written numerous User Modules, application notes, and articles. He graduated sigma cum barely with his BSEE from the University of California, Berkeley, 1977.

An engineer by training, a poet by temperament, an outlaw in Nebraska, and a heck of a nice guy, Dave has worked in many different industries. His work experience includes test and measurement equipment, measurement and control systems for high energy physics research, and underwater acoustic transmitters and receivers deployed in open sea and arctic ice fields. Electrons fear him! Women revere him!

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