

Equalize This !

Test Plan

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Version	2
Updates	<ul style="list-style-type: none">- Scope of work- Generic test setup- Test environment- Input pattern considerations- Resources- Appendices
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I. Scope of the work

The purpose of the series of tests to be performed in the context of “Equalize This!” is to characterize datacom appliances (equalizer, SerDes,...) under different condition of operations (data rate, pattern, input power, NEXT aggressor signal magnitude). The parameter used to quantify the performances of the Item Under Test (I.U.T.) being the jitter of the signal (Deterministic, Random, Total).

II. Testing

A. Description

Pattern generators are used to generate both the transmitted victim signal and the aggressor signal at the receiver side. The aggressor signal is introduced at the received side in order to emulate the NEXT effect. The aggressor signal is introduced on the connector pin that corresponds to the worst case NEXT. The introduced aggressor should be in phase with the received victim signal at the receiver side. The pattern length as well as the bit sequence of both the victim and aggressor signals can be changed. Further more, their amplitude can be varied. The victim after passing through the backplane is input into the Equalizer to test its performance in terms of Jitter and BER.

B. Generic test setup

Following is a schematic of the generic test setup (Figure 1). The I.U.T. is a datacom appliance with binary signal at the input and binary signal at the output. The signal sent over the backplane can be of any nature (binary, multi-level). The I.U.T. can be a transceiver or a simple equalizer. In the case of a simple equalizer the I.U.T. is reduced to the Rx part shown on the path of the victim channel of the generic test setup.

The high frequency oscilloscope can be used to monitor the actual waveform, and the error detector is used prior to testing to verify the proper operation of the I.U.T. The Jitter Analyzer is used to characterize the performance of the I.U.T. under different condition of operations.

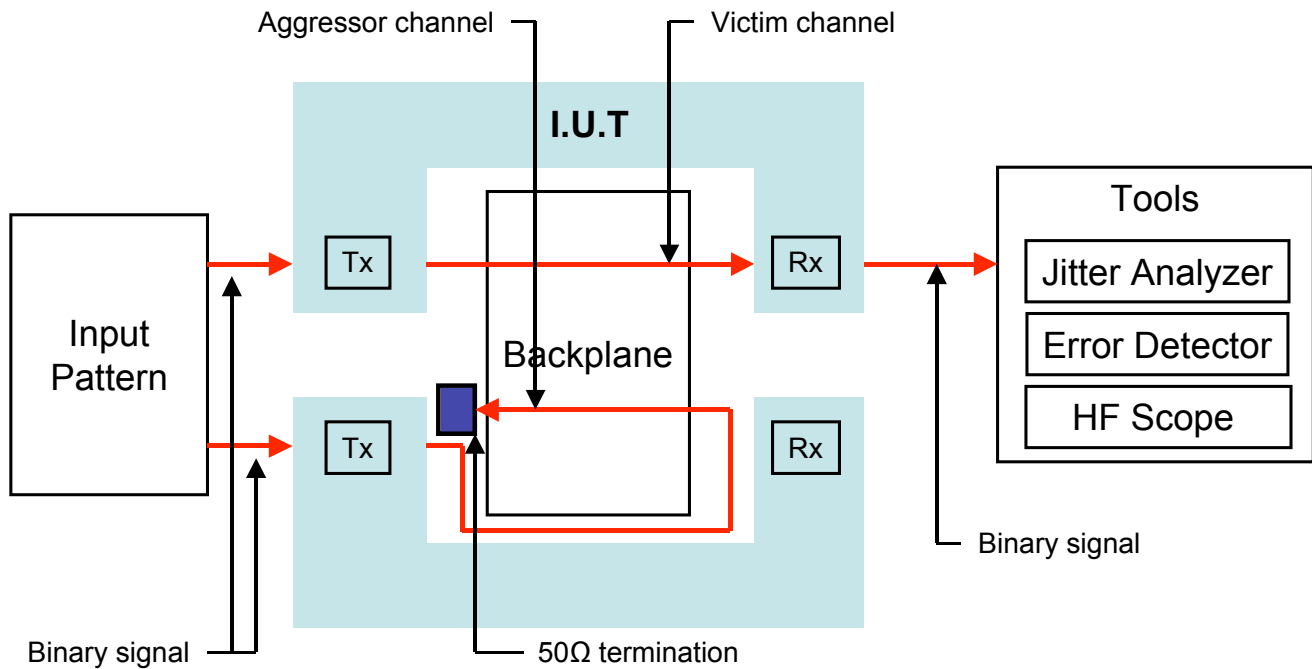


Figure 1: Generic schematic of the test setup

C. Test environment

The datacom appliances will be tested under different condition of operations (data rate, pattern, input power, NEXT aggressor signal magnitude...).

a. Backplanes

The currently available backplanes are:

- Tyco HM-Zd test backplane (2, 16, 30 inches);

b. Signal test patterns

The following test patterns will be used:

- K28.5: Mixed frequency test pattern for testing DJ ($2^{11}-1$);
- PRBS11: Pseudo-Random-Bit-Sequence testing;
- CJTPAT: Continuous Jitter Test Pattern.

c. Signal amplitude

The amplitude of the signal to test the I.U.T. will be determined from the datasheet of I.U.T., within accessible values (see “D. Input pattern considerations”).

d. Signal data rate

The data rate of the signal applied to a specific I.U.T. will be determined from the I.U.T. datasheet, within accessible rate of the pattern generators.

e. NEXT aggression

A single NEXT aggressor will be consider for the testing of the I.U.T.. The worst case NEXT aggressor is determined for the considered backplanes, within the accessible channels from the daughter card, from differential S-Parameter measurements.

f. NEXT aggressor amplitude

The amplitude of the NEXT aggressor will be x_0 , x_1 and x_2 of the signal magnitude, if within the accessible values of the pattern generators (see “D. Input pattern considerations”).

D. Input pattern considerations

There are different ways to feed the input binary signals into the I.U.T.:

- a. one pattern generator is used per input; in this case all the signals are independent, and their respective amplitude can be controlled more precisely and with more flexibility. This situation represents a real world mode of operation.
- b. one pattern generator is used for more multiple inputs; in this case, all the signals are not independent, and their respective amplitude are ratios determined from broadband attenuators, resulting is less flexibility and reduced amplitude range.

Falling under situation a) or situation b) depends on the equipment availability. Figure 2 illustrates different input signal generation.

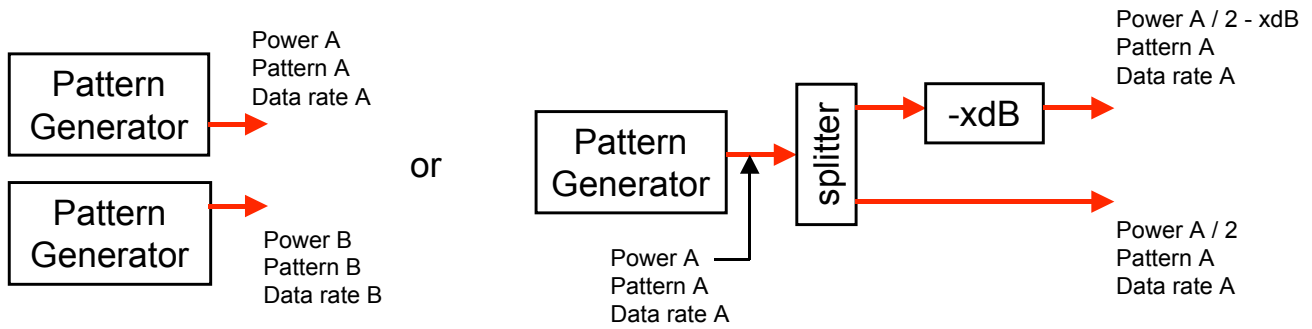


Figure 2: Illustration of the different signal generation scheme.

E. Data to be provided

In the context of “Equalize This!”, all the measurements will be achieved with and without an aggressor channel at the receive side of the link to emulate the NEXT effect. The input PIN of the aggressor will be selected within the accessible PINs to simulate the worst case NEXT. The aggressor channel is x_0 , x_1 and x_2 in magnitude the victim channel input power level. The quantitative parameter to evaluate the performance of an I.U.T. is the jitter for a given BER. The variables being the backplanes, the channel length, the input power levels, the data rates and the pattern sequence. In addition to the jitter, power consumption of the I.U.T. is monitored.

More specifically the measurements are:

- Deterministic Jitter versus channel length for different:
 - Input power levels (0.5 up to 1.6 V) at a fixed pattern ($2^{11}-1$) and data rate;
 - Pattern Sequence (K28.5 and $2^{11}-1$, and CJTPAT) at fixed input power and data rate;
 - Data rate (up to 6Gbps) at a fixed input power and a fixed pattern ($2^{11}-1$);
 - NEXT aggressors (0x, 1x and 2x) at fixed input power, pattern ($2^{11}-1$) and data rate.
- Random Jitter (10^{-12} BER) versus channel length for different:
 - Input power levels (0.5 up to 1.6 V) at a fixed pattern ($2^{11}-1$) and data rate;
 - Pattern Sequence (K28.5 and $2^{11}-1$, and CJTPAT) at fixed input power and data rate;
 - Data rate (up to 6Gbps) at a fixed input power and a fixed pattern ($2^{11}-1$);

- NEXT aggressors (0x, 1x and 2x) at fixed input power, pattern ($2^{11}-1$) and data rate.
- BER versus Total Jitter for different:
 - NEXT aggressors (0x, 1x and 2x) at fixed input power, pattern ($2^{11}-1$), data rate and channel length.

The above-mentioned data (per I.U.T.) are provided 2 weeks after reception of the I.U.T..

F. Resources

a. Backplanes

From a channel perspective, GeorgiaTech has:

- HM-Zd Test Backplane (Tyco): 2", 16" and 30";

And GeorgiaTech is expecting from Teradyne, via Lee Goldberg:

- VHDM 10 and 20 inches including new (HST) and older connector version;
- HSD and GBX, 6,18,24 and 30inches.

b. Hardware

From a measurement equipment perspective, GeorgiaTech has:

- Jitter Analyzer (Wavecrest SIA-3000, up to 6GHz);
- Pattern generators / Error detector:
 - Agilent BitAlyzer (3.6Gbps);
 - Anritsu MP1763A / MP1764B (12Gbps);
 - Agilent 71612B 12Gb/s Error Performance Analyzer (12.5 Gbps) –
Reduce access to this equipment.
 - Advantest (10Gbps) – *Reduce access to this equipment.*
- Miscellaneous (power supply, cables, scope...)

Equipments we need to buy:

- Pattern generators:
 - LA19-02-01 12Gbps pulse pattern generator;

Equipments we may need to buy/loan/rent (related to the type of I.U.T. that will be sent to GeorgiaTech):

- Pattern generators:
 - 16 x 622Mbs pattern generator.

c. Man power

The measurements will be performed/monitored by Dr S. Nuttinck. He will be assisted by (from GeorgiaTech):

- 1) Soumya Chandramouly
- 2) Rajarshi Mudhopahay
- 3) Hyoungsoo Kim

III. Appendices

A. Comments from John D'Ambrosia at Tyco

Test plan comments from John D'Ambrosia 7-15-03

Note = forward Quellan review to John

At 3.125G no pattern generator can represent real-world signal and spectral content – something like an Ixia box or Spirent TRAFFIC generator would produce more realistic conditions. Or, anybody's SerDes (Marvell)

The test plan does not clearly explain that EQ circuits need to be paired with transceivers for tests.

There is concern that backplanes in use for test may not represent equivalent channel conditions. Efforts must be made to a) make sure we don't get overly- "sweetened" boards that make the mfr look good, and b) the supplier will answer a questionnaire about how the boards were designed and manufactured. Tyco strongly suggests we select and use channel sets within the boards we use that represent best, worst, and average conditions. The manufacturers would probably be very helpful here. It is strongly suggested that for the majority of tests, the "worst" channel pairs on each backplane be used.

When introducing aggressor channels, the test plan is not clear precisely where the adjacent victim signal will be in relation to it. This varies between connectors – need clarification. Easy solution would be to state that you will use the "worst case" aggressor pair for a given connector, determined by frequency sweeps.

The description of the speed classes is a bit misleading, and does not indicate that each device is run to test max and min useful speeds. This is just a semantic issue but should be clarified.

The patterns specified are not "worst-case" or representative patterns. Suggest using CJPAT and possibly 2³¹. 2³¹ is not appropriate for XAUI, but does occur in SONET. No clue about what's worst-case for MLT, but Accelerant (Bill Hoppin) may be a good source for this information.

B. Comments from Lee Harrison at KeyEye

Test plan comments from Lee Harrison at KeyEye 7-15-03

Lee:

Mike gave a copy of the plans for the Equalize This! Challenge. It looks great and I wish our silicon was going to be out of the fab by then but we will not have anything until mid-October. After reading the proposal, I did have a couple comments though that may or may not be useful. I read through the descriptions of the boards and it looks like you are using the Tyco demo boards that have been used in the past. These are good boards for apples to apples comparisons but have been seen to be very optimistic in terms of actual "real-world" performance. The routing used was much less intense than what you will see in an actual routers or switches. There are fewer vias and better matching. They also have used better connectors. I could not tell if these were the FR-13 boards I have seen data in the past or GTEK. However, for newer designs this might be fine. I did see you are putting together a legacy board. It would be nice to have this use some cheaper connectors and standard FR-4. Even though you called this legacy this is the material people would still like to use if they can. It is cheap and they know how to manufacture it in volume. It will be interesting to see how people perform on this.

I also noted that you are planning to use only one aggressor. Most of the crosstalk comes from the connector but it is not always straight-forward to see which aggressor will cause the most crosstalk. In fact, it is often not the one you think because of the fact a big issue turns out to be the barrels beneath the connector in some cases that is the culprit. Another issue is the trace length matching in the connector bend which can cause differential to common mode conversion problems. I would highly recommend using multiple aggressors surrounding the victim. This guarantees that you will get what you need to see. I think that if we pick better materials, space traces properly with simple routing, and use better connectors we all could go much faster. This is not what an OEM designer faces. You will not have to go very far to find one high-speed SERDES company who did multiple demos and announcements at the last DesignCon and then when their part was placed in real designs at multiple OEMs this year they failed miserably.

Lastly, it looks like you have a variety of people who want to go to 10Gbps or above. Great! If you pick ideal conditions you can get this to work. However, the real issue is that people have thousands of cards based on last generation SERDES. Try one experiment where you use XAUI on the alternate channels and monitor their BER as you run the higher speed SERDES in the same connector. You will be surprised at what you see.

Good luck and if we can be of any help let us know.

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Lee

Lee Harrison, Vice President
KeyEye Communications, Inc
lee.harrison@keyeye.net
Phone: 916-362-6440, Cell 916-804-1490

C. Emails about the Teradyne backplanes

From: "Lee Goldberg" <lgoldberg@green-electronics.com>
Date: Tue Jul 15, 2003 03:27:08 PM US/Eastern
To: <MeaganMorrell@notes.teradyne.com>, "Sebastien Nuttinck" <sn46@prism.gatech.edu>
Subject: RE: Backplanes - GeorgiaTech

Hi Meagan -

I hope it's OK for me to jump in here and reply for Sebastien, I normally don't do this but a large delay could prove to be a problem for us and I wanted to help straighten this out as soon as possible.

First, I want to say I really appreciate you being up front with us about a possible delay - it is much, much better than waiting around wondering why the backplane is not here. Given the crazy nature of this business, I'm not surprised that we might hit a delay like this, and quick actions on your part will help a small problem from becoming a disaster.

One thing that would help us figure out if there is a problem at all is if you can clarify the term "a few weeks". If this means 2-3 weeks on the outside, we can most certainly live with this without a second thought. If you're talking much more than this, it could start to impact on our test program. The good news is that if we know when to expect it, there may be ways to design our schedule so that we can work around the missing article until it arrives.

In either case, a slightly better idea of how long the anticipated delay will be would help tremendously. Of course, anything you can do to get a backplane into our hands in 2-3 weeks would help even more, but we will certainly understand if this is not possible.

Please let me know if there is anything I or GA Tech can do to work with you on this, or any other issue.

Best,

LEE

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-----Original Message-----

From: Sebastien Nuttinck [<mailto:sn46@prism.gatech.edu>]
Sent: Tuesday, July 15, 2003 2:28 PM
To: lgoldberg@green-electronics.com; Chris Evans; Edward Gebara; Joy Laskar
Subject: Fwd: Backplanes - GeorgiaTech

FYI, about teradyne backplanes.

Seb.

Begin forwarded message:

From: MeaganMorrell@notes.teradyne.com
Date: Tue Jul 15, 2003 02:03:35 PM US/Eastern
To: Sebastien Nuttinck <sn46@prism.gatech.edu>
Subject: Re: Backplanes - GeorgiaTech

Hi Sebastien,

I just wanted to give you a heads up that there is going to be a slight delay in getting these boards to you. I currently don't have any loaded with connectors which I have to do and I am booked right now with other projects. I am expecting to be able to get these to you within a few weeks. Please let me know if you are in any particular hurry for them.

Thanks,
Meagan

Sebastien Nuttinck <sn46@prism.gatech.edu> on 07/10/2003 03:39:54 PM

To: meagan.morrell@teradyne.com
cc:

Subject: Backplanes - GeorgiaTech

Greetings meagan,

following is the address where to send the backplanes:

Sebastien Nuttinck / Chris Evans
TSRB Building
85 Fifth Street, N.W.
Atlanta 30308

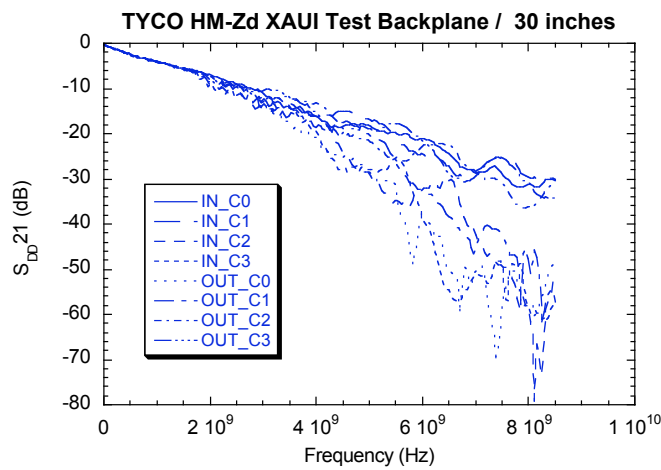
Thank you, Best regards, Sebastien.

D. Worst NEXT case: HM-Zd Tyco, 30 inches

Available pins/channel from daughter card:

TB				IN_C3	OUT_C3		T2
				IN_C2	OUT_C2		
				IN_C1	OUT_C1		
TA				IN_C0	OUT_C0		T1

Worst transmission: OUT_CO and IN_C3



NEXT on IN_C3:

