

Designing Multi-Gigabit Serial Backplanes with High Speed SERDES Solutions

Marketing White Paper

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Granted

The technology discussed in this document is protected by one or more of the following patent grants:

U.S. Patent No. 6,316,977. Other relevant patent grants may also exist.

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1 Introduction

Old design “rules of thumb” are no longer valid for multi-gigabit backplane design involving high speeds and fast edge rates. For years, backplane-based systems evolved by moving to wider buses and faster signal clock rates. However, when designs reached the 1 Gbit/s range, it became impossible to pass data reliably over parallel buses because signal skew and load problems increased. Designers were forced to shift from parallel buses to serial interconnects. Using silicon serializer-deserializer (SERDES) solutions, backplanes can utilize a serial stream that combines data and clock in the same signal.

At data rates beyond the 1 Gbit/s level, new problems arise that backplane designers have to compensate for. The signal integrity of these high-speed serial links is affected by reflections due to impedance mismatches along the signal path, signal attenuation from backplane materials, added noise due to crosstalk and Inter Symbol Interference (ISI). As networking, computing and storage applications are driving line card data throughput requirements to 40 Gbit/s and beyond, signal integrity is more critical than ever.

Today, state-of-the-art systems typically run data rates of 3.125 Gbit/s across 20 inches or more of backplane trace. Next generation high-end applications are looking at rates of 6.25 Gbit/s and beyond.

Fortunately, a backplane designer can reduce the effects of the signal degradation phenomena by choosing appropriate board materials and applying proven techniques for high-speed board layouts¹. In addition, the signal integrity of a multi-gigabit serial link can also be improved by the appropriate choice of SERDES device. A SERDES device with integrated termination resistors, programmable output swing, transmit pre-emphasis and receive equalization, such as PMC-Sierra’s PM8355 QuadPHY-II™ device, can reduce the effects of impedance mismatch and attenuation, resulting in improved signal integrity and a low Bit Error Ratio (BER).

¹ See PMC-Sierra’s Application Note PMC-2010750 Issue 3, *Signal Integrity For PMC-Sierra’s 3.125/2.488/1.5Gbps Links*, for detailed guidelines on designing high-speed backplanes.

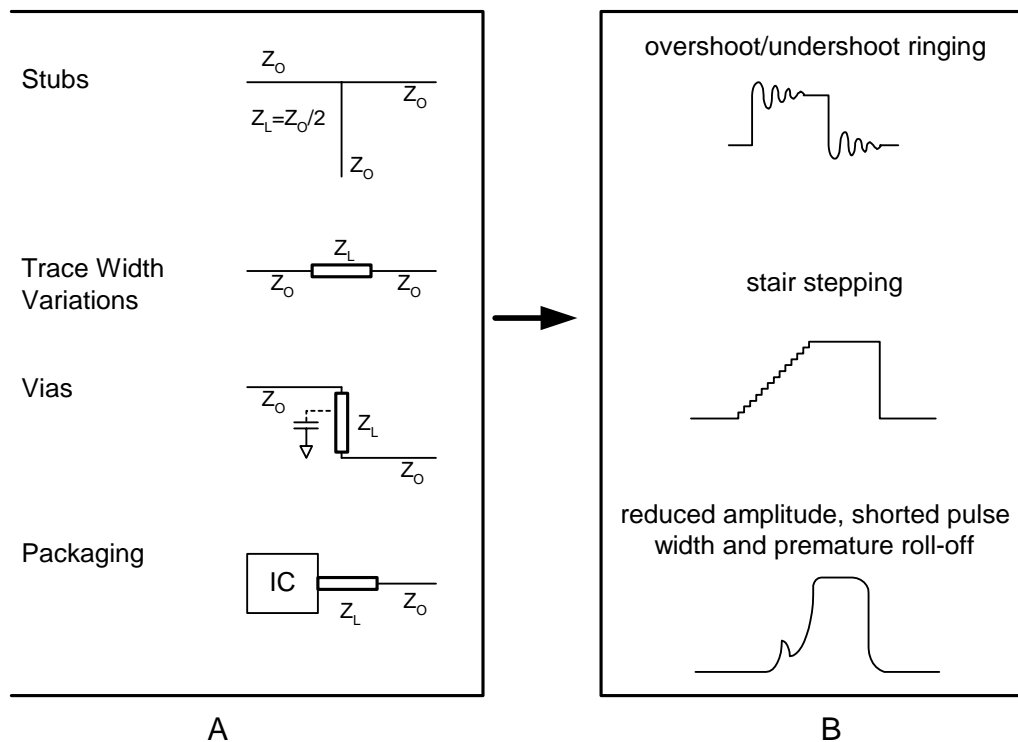
2 Backplane Design Challenges

2.1 Reflections

In the past, devices that drove backplane traces usually had signal edge rates that were more than twice the period it took for the wave to propagate through the trace. In these cases, simpler lumped element models were valid. However, at higher speeds transmission line effects dominate.

Impedance mismatches between a device driving a transmission line, the line itself, and the far end terminations can result in large reflections on the line and degrade performance. These effects will appear as overshoot, undershoot, ringing, or stairstep waveforms on the trace if the load or the driver are improperly matched, as shown in Figure 1. For high performance designs, matching is required. The ideal transmission line matches the impedance of the driver and the impedance of the load equals the characteristic impedance of the trace. In this case, the maximum power of the driving device will be transferred to the load.

Figure 1 (a) Impedance mismatches that can occur on a printed circuit board. (b) Signal impairments introduced by the impedance mismatches.



A terminating resistor can be added to reduce or eliminate unwanted reflections on a transmission line and assure the best quality signals. The resistor can be placed external to the device or integrated into the silicon circuit. With an integrated termination resistor, the signal quality is improved as a result of terminating closer to the end of the transmission line than would be possible externally. In addition, an integrated termination resistor can have a lower parasitic capacitance and inductance than an external resistor. A figure of merit for a device's ability to reduce unwanted reflections is measured as return loss. Return loss characterizes the amount of reflected energy when a signal is applied to the device. A higher return loss implies lower reflected energy, which is the desired performance. .

The QuadPHY-II™ device has integrated termination resistors at the high-speed transmit and receive interfaces and meets the IEEE 802.3 10GE specification for return loss. This high level of integration reduces transmission line reflections by eliminating discontinuities caused by unterminated stubs in the high-speed signal path. In addition, the integrated resistors decrease the external component count resulting in space savings and a lower bill of materials (BOM) when several serial links are integrated on to one chip.

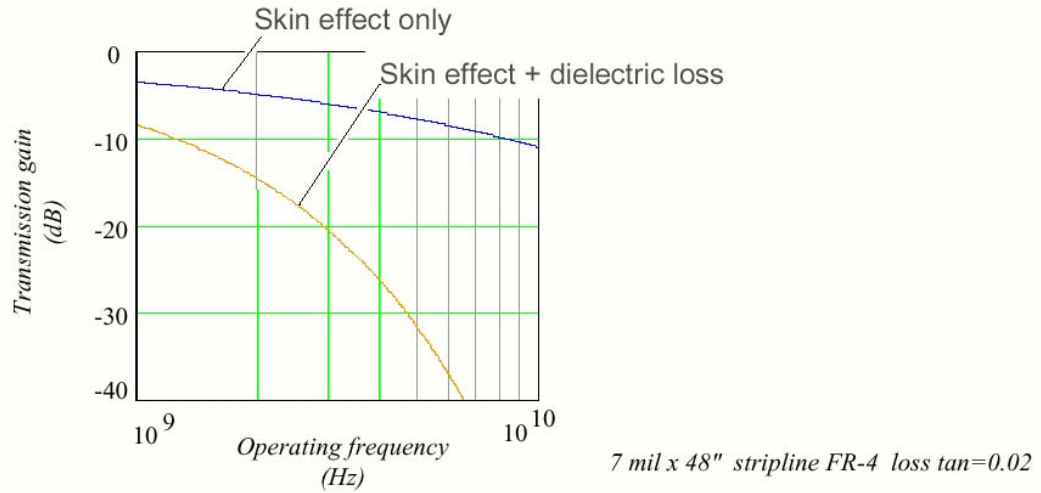
2.2 Crosstalk

Another factor impacting signal quality in multi-gigabit backplanes is crosstalk, the noise related to the coupling of signals on parallel transmission lines at the near end or far-end of the line or trace. Crosstalk arises from coupling on the PCB, both in the line card and the backplane, inside the package and within the backplane connectors. Crosstalk can be categorized as either Near-End or Far-End Crosstalk (NEXT and FEXT), with NEXT being much larger in amplitude than FEXT. In either of these categories, the amount of crosstalk is dependent upon signal amplitudes, signal spectrum, and trace/cable length. At higher bandwidths, these factors dominate and increase the error rate of the transmission. Being able to control the transmit amplitude of a device helps minimize the effects of FEXT and NEXT noise. Using only the minimum transmitter amplitude to achieve reliable BER operation of a system will reduce the effects of crosstalk. In addition, providing integrated termination resistors on the transmitter output helps to squelch NEXT. The QuadPHY-II™ device has three programmable output swing levels and integrated termination resistors on the transmitter to help reduce the effects of crosstalk.

2.3 Attenuation

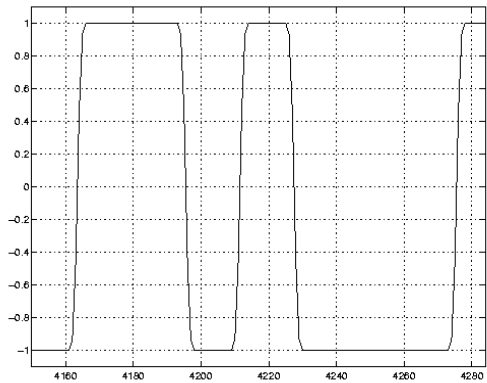
High-speed signals transmitted across a backplane will experience signal attenuation due to the skin effect and dielectric losses. The skin effect describes the phenomena of high frequency current traveling in the outer "skin" of a conductor, increasing the resistance to the flow of current. The skin effect is caused by the self-inductance of a conductor, which causes an increase in the inductive reactance at high frequencies and forces the electrons toward the surface of the conductor. Thus, the high frequency component of the signal is attenuated. At low frequencies, from 1.25 to 2.5 Gbit/s, skin effect and dielectric losses are equal contributors to signal attenuation. However at frequencies greater than 2.5 Gbit/s, dielectric losses begin to dominate as shown in Figure 2.

Figure 2 Attenuation in a 48" FR4 PCB Channel (Source: Howard Johnson)

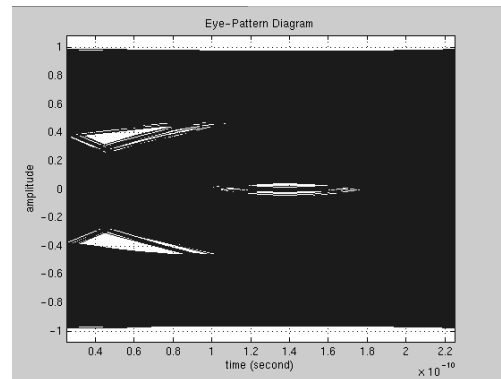


An open eye at the transmitter can be closed at the receiver after it has passed through a backplane due the combination of skin effect and dielectric losses, as shown in Figure 3.

Figure 3 Example of a Non pre-emphasized signal, (a) Non pre-emphasized output at the transmitter (b) Closed eye seen at the receiver after 30" of backplane trace



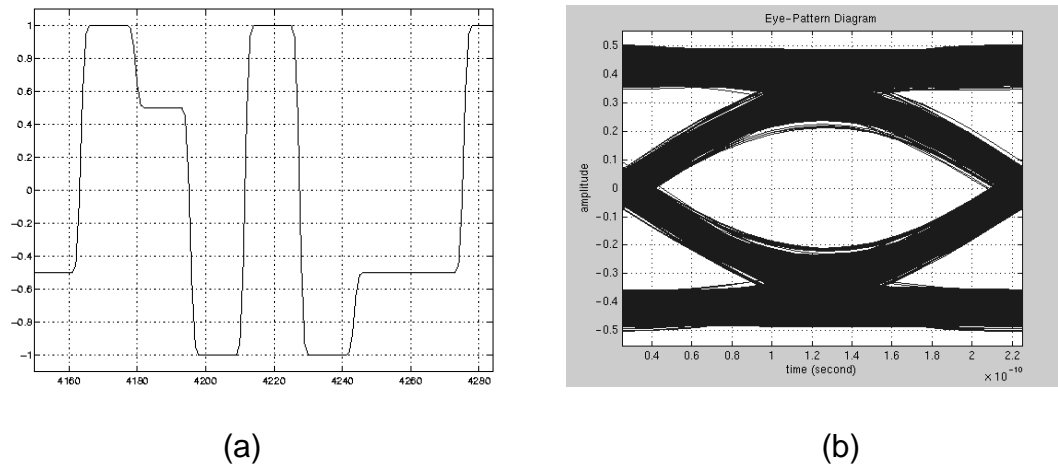
(a)



(b)

Pre-emphasis is one technique that is used to combat eye closure due to high frequency attenuation. Pre-emphasis boosts the higher frequency components of the signal, counter-acting the high frequency attenuation of the backplane traces. At the transmitter, the high-frequency components of a signal are accentuated, or emphasized, so that by the time the signal reaches the receiver, via a PCB channel, the high frequency portion will be attenuated to the desired level. A pre-emphasized signal at the output of a transmitter is displayed in Figure 4(a). After the signal travels through the backplane and is attenuated, the receiver sees an eye that is shown in Figure 4(b).

Figure 4 Example of pre-emphasized signal, (a) Pre-emphasized signal at the transmitter output (b) Open eye seen at the receiver after 30” of backplane trace.



The QuadPHY-II™ device has selectable transmit pre-emphasis. In applications with short backplane traces or intra-board traces, the pre-emphasis can be disabled. However, when driving longer backplane lengths, pre-emphasis can be enabled to ensure an open eye at the receiver and a low BER. The QuadPHY-II™ device’s pre-emphasis has been tested to transmit data error-free on traces up to 60”in length on FR4 backplane material.

Pre-emphasis has become a mature technology and most of the existing 10 Gbit/s SERDES chips employ it. While some argue that pre-emphasis alone is a sufficient solution, there is another set of problems, such as Inter Symbol Interference (ISI), which pre-emphasis only partially resolves at higher speeds. To tackle ISI at high frequency, a SERDES device must incorporate receiver equalization. Unfortunately, most transceivers only offer pre-emphasis as a means to combat the signal degrading effects associated with high-speed backplane designs.

2.4 Inter Symbol Interference (ISI)

Inter Symbol Interference or ISI is the spreading and smearing of symbols such that the energy from one symbol degrades subsequent symbols causing the received signal to have a higher probability of being interpreted incorrectly. ISI can be caused by many different phenomena and is an unavoidable consequence of both wired and wireless communication systems. ISI can be caused by: filtering effects from hardware, frequency selective fading, non-linearities and/or charging effects. Very few systems are immune to ISI, and any high-speed communication system designs must incorporate techniques for controlling the impact of ISI.

As mentioned earlier, pre-emphasis alone at the transmitter does not effectively address the problem of Inter Symbol Interference. Pre-emphasis helps to reduce ISI by providing some high frequency boost, but it has little effect on the frequency spectrum beyond (data rate)/3. Using a receive equalizer provides a frequency boost beyond what pre-emphasis can do, completely eliminating the effects of ISI.

At slower signal rates, pulse widths are long and can be sampled far from the signal boundaries to avoid the symbol overlap. At faster rates, ISI becomes a more severe problem. Approaching 10 Gbit/s, ISI is no longer apparent only at the signal boundary and it starts to affect the whole width of the bit. Using equalization, the transceivers can be tuned to minimize the effects of ISI. The key benefit of receive equalization is that it improves receiver performance without increasing the peak transmitter power.

Equalization at the receiver can be designed using either analog or digital (DSP-based) methods. The digital or DSP-based solutions use analog to digital conversion and digital filtering for equalization. The analog approach uses linear filter circuits to equalize the attenuated signals. The QuadPHY-II™ device has programmable analog receive equalization to minimize the effects of ISI. The programmable equalization paired with the selectable pre-emphasis of the QuadPHY-II™ device allows designers to fine-tune the signal integrity performance to their unique backplane environment.

3 PMC-Sierra's QuadPHY-II™ Device

PMC-Sierra's flagship PM8355 QuadPHY-II™ device offers the industry's widest range of 10 Gigabit backplane operation, from 1 Gbit/s to 3.125 Gbit/s, while supporting IEEE 802.3ae 10 Gigabit Ethernet Standard, Fiber Channel and Infiniband (2.5 Gbit/s) optical applications. As a 10 Gigabit Ethernet PHY, the QuadPHY-II™ device supports the 10 Gigabit Attachment Unit Interface (XAUI) and Coarse Wavelength Division Multiplexing (CWDM) optical module serial interfaces. It also provides a standard XGMII parallel interface for seamless connection to 10 Gbit/s Media Access Controllers (MACs). Its per-channel selectable half-rate mode can support either 1.06 Gbit/s or 2.12 Gbit/s Fiber Channel rates on each port independently.

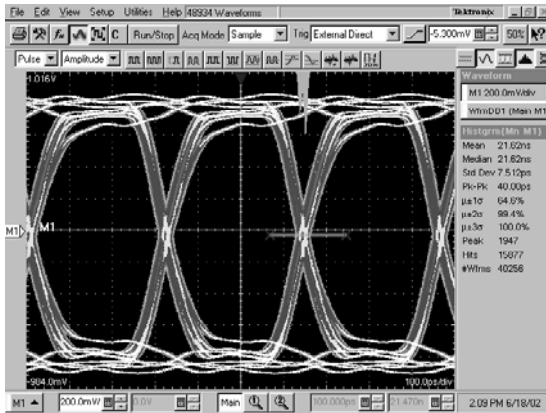
The QuadPHY-II™ device integrates four independent transceivers operating at up to 3.125 Gbit/s each with integrated serializer/deserializer, clock synthesis, clock recovery and 8B/10B encode/decode logic. The QuadPHY-II™ device also has a half rate mode that is selectable on a per-channel basis. The 10-bit Dual Data Rate (DDR) parallel interface has selectable source-simultaneous or source-synchronous transmit and receive parallel interfaces and a convenient output clock for user-friendly ASIC timing. The DDR interface interoperates with both 1.8V LVCMOS and the 2.5V SSTL_2 interface standards for ease of interfacing to new or legacy ASICs. The QuadPHY-II™ device also features an integrated receive FIFO to synchronize incoming data to the local clock domain and a trunking feature to de-skew and align all four channels to form a single 10 Gbit/s logical link.

The high speed serial I/Os have programmable equalization, selectable pre-emphasis, variable output swing selection and integrated termination resistors. Each of these features minimizes the challenges associated with high-speed backplane design, providing robust 3.125 Gbit/s serial link operation. In addition, the QuadPHY-II™ device has redundant high-speed serial I/O channels for convenient protection switching to a redundant fabric.

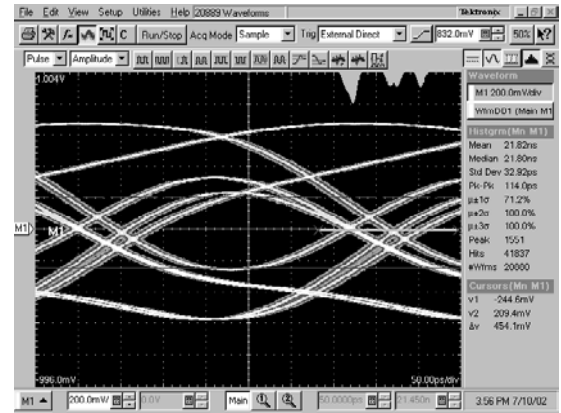
The QuadPHY-II™ device has been verified to meet industry standards for 10 Gigabit Ethernet by successfully participating in several interoperability events including: University of New Hampshire Interoperability Laboratories, and 10 Gigabit Ethernet Alliance sponsored interoperability events at N+I and Supercomm. The QuadPHY-II™ device has interoperated successfully with several XENPAK vendors, including Agilent, JDS Uniphase, Optillion and many others. The QuadPHY-II™ device has a proven BER of better than 10^{-15} over a 30" trace and two backplane connectors comprising the 10GEA XAUI Interoperability backplane designed by TYCO Electronics. This surpasses the 10 Gigabit Ethernet standard BER and backplane trace length specification of 10^{-12} BER over 20" of backplane trace.

To demonstrate the QuadPHY-II™ device's performance, the IEEE 802.3ae compliant continuous jitter test pattern, CJPAT, is transmitted from the QuadPHY-II™ device across a 30" TYCO XAUI Backplane. The CJPAT test pattern, called out in the 10 GE specification, is used for jitter compliance testing and is meant to stress the receiver clock recovery circuit. The 30" TYCO XAUI backplane is a 10GE industry-recognized backplane designed for interoperability testing. The resulting eye diagrams (shown in Figure 5) are taken at the transmitter output and the receiver input after 30" using the CJPAT pattern. In this set of measurements, the QuadPHY-II™ device is configured to transmit and receive the CJPAT pattern without pre-emphasis. With no pre-emphasis, the vertical eye opening after 30" of backplane trace at the receiver is 454mV and the peak-to-peak jitter is measured as 114ps.

Figure 5 Without pre-emphasis (a) CJPAT eye diagram at the transmitter output without pre-emphasis (b) CJPAT eye diagram at the receiver after a 30” backplane trace on the TYCO XAUI Interoperability Platform



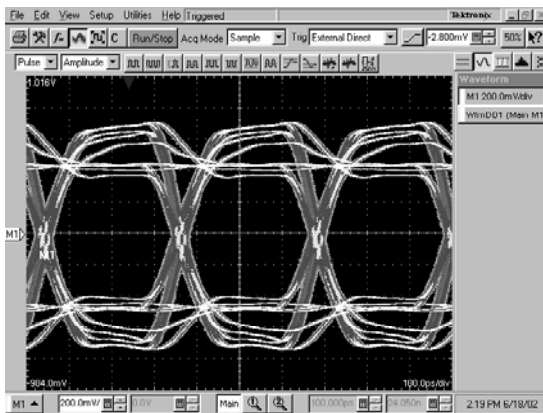
(a)



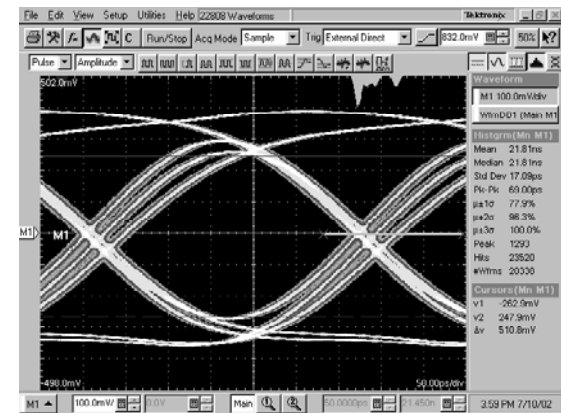
(b)

Enabling pre-emphasis on this link, the resulting eye diagram at the transmitter and receiver are shown in Figure 6. Using pre-emphasis opens the receiver eye by 60mV and reduces the jitter by 45ps on the same 30” backplane trace with CJPAT data pattern. In this configuration, the QuadPHY-II™ device has achieved a BER of greater than 10^{-15} over 30” of FR4, exceeding the IEEE 10GE standard BER of 10^{-12} over a 20” backplane trace length.

Figure 6 With pre-emphasis (a) CJPAT eye diagram at the transmitter output with pre-emphasis (b) CJPAT eye diagram at the receiver after a 30” backplane trace on the TYCO XAUI Interoperability Platform



(a)



(b)

4 Summary

In multi-gigabit backplane designs, several factors can contribute to degraded signal integrity including reflections, crosstalk, attenuation and ISI. These factors can be mitigated by the proper choice of a backplane SERDES. The QuadPHY-II™ device has integrated termination resistors, programmable output swing, selectable pre-emphasis, and programmable equalization. Each of these QuadPHY-II™ device features reduces, and in some cases eliminates, the signal integrity degrading effects that are inherent in transmission lines.

The QuadPHY-II™ device has been proven by interoperability testing to be a robust backplane SERDES solution compliant with the IEEE 802.3ae 10 GE specification. In addition, evaluating the jitter performance of the QuadPHY-II™ device across the industry standard TYCO XAUI Interoperability Platform yields superior jitter results. The low power, small form factor of PMC-Sierra's QuadPHY II™ device, coupled with its unparalleled signal integrity performance, make it the optimal choice for multi-gigabit backplane designs.

Notes