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White Paper

High Performance Backplane Design Using the Marvell Alaska™ X Quad 3.125 Gb/s SERDES

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Introduction

With the introduction of communications systems such as high-end routers and switches that are capable of handling several hundred Gigabits per second to Terabits per second of bandwidth, robust backplane design becomes more important than ever before. Backplanes based on serial transmission and copper medium are typically the solution of choice for this class of communication systems due to several advantages compared to other techniques such as backplanes based on parallel buses and optical signals. The key advantages of copper backplanes are reduced cost, superior reliability and lower complexity.

- Reduction in cost results from elimination of expensive optical components.
- Optical components pose reliability problems due to their active nature as opposed to copper backplanes which tend to be of passive nature.
- Net reduction in number of components results in overall lower complexity.

Although copper backplanes offer significant advantages, they do come with their own challenges. Some of the key challenges are higher attenuation and signal integrity.

Higher Attenuation

At Gigabit per second and higher speeds, skin effect becomes a prominent factor in signal transmission over long backplane traces along with the inherent dielectric losses in the system. Typically, FR4 laminates have high dielectric loss at Gigahertz frequencies. FR4 is the most commonly used material for backplanes. In addition to skin effect and dielectric loss, connector loss also becomes significant at these frequencies. Overall, these various types of losses cause severe signal degradation in copper backplanes.
Higher frequency components of the signal are more adversely affected than lower frequency components due to the low pass nature of the transmission channels. This results in an “eye-closure” at the receive end. A smaller eye opening makes signal reception and recovery difficult for the receiver, which usually results in high Bit Error Rate (BER). High BER causes packet loss and reduced effective bandwidth. Figure 1 shows the frequency response of the IEEE 802.3ae 10 Gigabit Ethernet standard channel. The channel is characterized by the following equation:

$$\left|s21(f)\right| \leq -20\cdot\log(e)\cdot\left(a1\cdot f^{0.5} + a2\cdot f + a3\cdot f^{2}\right)$$

where f is frequency in Hz, $a1=6.5\text{x}10^{-6}$, $a2=2.0\text{x}10^{-10}$ and $a3=3.3\text{x}10^{-20}$. s21 is the “s-parameter” for transmission magnitude response. The response shows low pass nature of the channel.

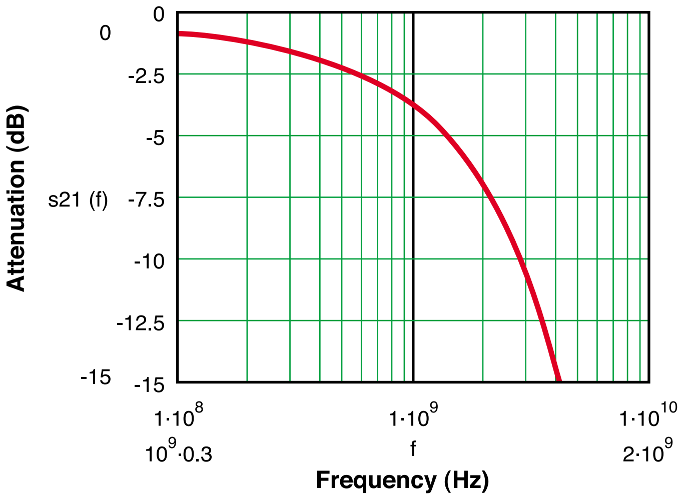


Figure 1: Channel response from IEEE 802.3ae

The IEEE channel corresponds to a typical backplane design with a total of only 20 inches of FR4 traces. In many cases, the backplane requirements may be more stringent than the IEEE specification thereby requiring higher performance design. An example of such a requirement is operation over longer links that involve up to 40 inches of traces.

Signal Integrity

In addition to higher losses, BER is significantly affected by various factors that contribute to degraded signal integrity or poor signal-to-noise ratio. Impedance mismatch is the main mechanism for this type of signal degradation. Impedance mismatch causes signal degradation by causing reflections. Typically, the impedance mismatch is caused by manufacturing or design problems such as over-etching, poorly designed vias and lack of perfect connector to board impedance matching.

Higher attenuation and poor signal integrity problems can be mitigated to a great extent by using improved board design techniques, superior connectors and sophisticated signal processing techniques in the SERDES components. Board and connector issues are beyond the scope of this paper. The rest of this paper focuses on issues related to SERDES components in general, and signal processing aspects in particular.

There are two common forms of signal processing techniques used in multi-gigabit SERDES components for compensating for attenuation – a) transmit pre-emphasis and b) receive equalization.

Transmit Pre-Emphasis

In this form of signal processing, the energy in the high frequency portion of the spectrum is boosted at the time of transmission. Since, high frequency components are attenuated more than lower frequency components, an equalized eye results at the destination. This enables the receiver to recover signal easily. This technique is simple and effective for high data rate designs.

Receive Equalization

In this form of signal processing, the signal is transmitted without any special processing and is “equalized” at the receiver using filtering techniques. There are two main forms of such equalization techniques – analog and digital (DSP based). Analog techniques use linear filter circuits to equalize the attenuated signals whereas DSP based techniques use digital filters and analog to digital conversion for equalization.

Choice of the right equalization technique is heavily dependent on the application. Receive equalization is well-suited for certain applications such as 100BASE-T and Gigabit Ethernet over Category 5 UTP cables, whereas transmit pre-emphasis better serves the needs of backplane applications. This is due to the fact that the data rates in multi-gigabit applications are much higher than the Fast Ethernet or Gigabit Ethernet and the transmission is on PCB traces as opposed to UTP cable. Following are the advantages of transmit pre-emphasis in backplane applications.

Advantages of Transmit Pre-Emphasis

1. Lower power consumption – Typically, transmit pre-emphasis at multi-gigabit per second speeds is performed by current summation in the high-speed transmit current mode driver. This method results in a small power overhead compared to a normal driver without pre-emphasis. In contrast, receive equalization must use dedicated high power circuitry to perform the equalization. This power is in addition to the power dissipated in the current mode transmit driver.

2. Superior performance – For receive equalization, receiver bandwidth needs to be significantly higher than the baud rate to adequately equalize the signal. This typically requires exotic process

technologies with higher cutoff frequencies. In case of comparable CMOS process technologies using pre-emphasis and receive equalization, lack of higher cutoff frequency results in a lower level of equalization.

3. Interoperability – Most vendors for multi-gigabit SERDES components utilize transmit pre-emphasis method. This ensures interoperability between various vendors. In the case of transmitter with pre-emphasis and receiver with equalization, the link would work fine. However, if a transmitter does not have pre-emphasis, and the receiver does not support equalization, the link may not work with acceptable BER for long channels. Figure 2 illustrates the concept of pre-emphasis. The signal is boosted at every bit transition on both positive and negative sides.

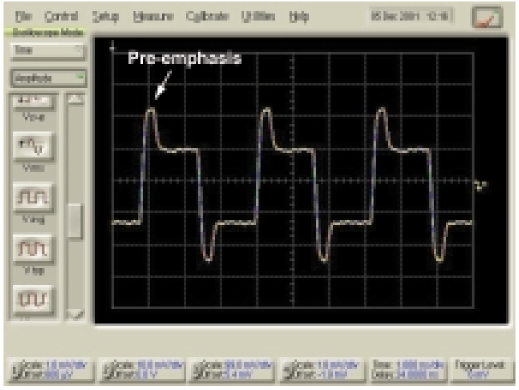


Figure 2: Illustration of pre-emphasis

The new Marvell quad 3.125 Gb/s SERDES, the Alaska™ X transceiver (88X2040), is specifically designed for 10 Gigabit Ethernet and serial backplane applications based on 4-channel operation up to 3.125 Gb/s. The Alaska X device features programmable transmit pre-emphasis and flexible clocking modes to support high-speed copper backplane applications based on the 10 Gigabit Attachment Unit Interface (XAUI) standard as well as proprietary implementations. The programmable output amplitude and pre-emphasis coupled with superior signal integrity allows the use of longer copper traces in excess of 60 inches with multiple connectors on generic low cost PCB materials such as FR4, lowering the overall system cost while providing system vendors with a forward migration path to higher throughput on existing backplanes.

Alaska™ X Transceiver Product Information

The Marvell Alaska™ X device, the 88X2040, is the industry's first 0.15 micron CMOS 10 Gigabit Ethernet 4-channel transceiver, which features the lowest power, superior jitter performance and smallest form factor solution on the market today. The Marvell Alaska X Gigabit transceiver is a fundamental building block of 10 Gigabit Ethernet systems. The 88X2040 transceiver incorporates all of the necessary functions to implement the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) functions as specified in the latest 10 Gigabit Ethernet IEEE 802.3ae draft, while achieving low power dissipation of 1.3 Watts.

The Alaska X device incorporates four transceivers operating up to 3.125 Gb/s, each with a selectable 8B/10B encoder/decoder. The four transceivers can operate at 1.0, 1.25, 2.0, 2.5, and 3.125 Gb/s to support a variety of backplane applications. Further, the Alaska X transceiver performs clock and data recovery and de-serialization for the receive path, as well as pre-emphasis, serialization and clock generation for the transmit path. The Alaska X device utilizes lower rate clocks as reference for internal clock generation. The device also allows for the use of either 62.5, 125 or 156.25 MHz reference inputs to provide flexible clocking.

The parallel interface on the Alaska X device is a 10 Gigabit Media Independent Interface (XGMII) as specified by the IEEE standard. In addition to the latest IEEE XGMII HSTL I/O support at 1.5V, the Alaska X transceiver features support for XGMII connection to legacy ASIC devices using HSTL I/O operating at 1.8V. For 10 Gigabit Ethernet applications, the device connects to optical modules such as the XENPAK using the XAUI interface and to 10 Gigabit Ethernet switch devices using the XGMII interface.

Several tests performed using the Alaska X devices and backplane connectors with various configurations of connectors and traces achieved BERs better than 10^{-15} over 60 inches of FR4 traces. This is several orders of magnitude better than the IEEE requirement of 10^{-12} BER for 10 Gigabit links. In addition to powerful amplitude and pre-emphasis control functions, the Alaska X device features lane-deskew capability, allowing for severe mismatch in trace length among the four channels. Eliminating the lane matching constraints removes a major bottleneck in dense backplane designs and provides greater overall flexibility in system design.

Following is an illustration of the Alaska X device’s superior signal integrity and pre-emphasis capabilities. Figure 3 shows a transmit signal without pre-emphasis.

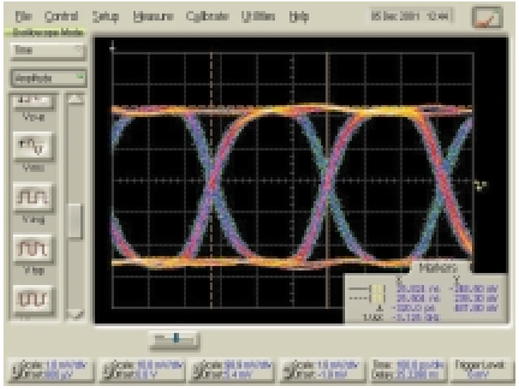


Figure 3: Transmit signal without pre-emphasis at 3.125 Gb/s

Figure 4 shows the effect of signal attenuation and connector losses through 40 inches of PCB traces on FR4 material with two backplane connectors and 4 SMA connectors. Note that the eye is significantly smaller compared to the transmit eye.

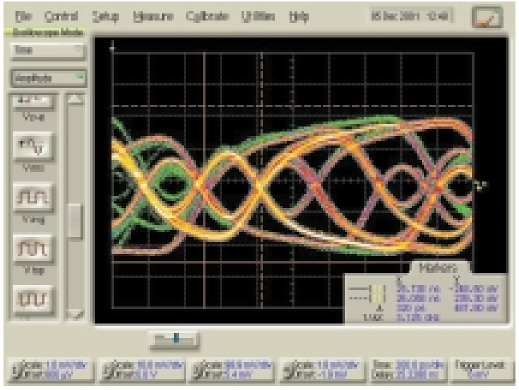


Figure 4: Receive eye after 40 inches of FR4 with 2 backplane connectors <u>without pre-emphasis</u> at 3.125 Gb/s

Figure 5 shows the 3.125 Gb/s transmit signal with pre-emphasis. The signal is intentionally distorted at the transmit end to get a clean eye at the receive end.

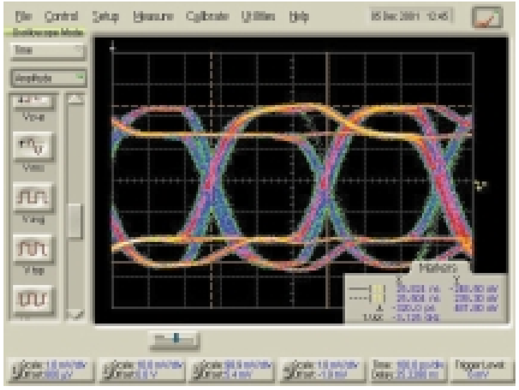


Figure 5: Transmit signal with pre-emphasis at 3.125 Gb/s

Figure 6 shows the effect of pre-emphasis on the receive eye with the same setup as Figure 4.

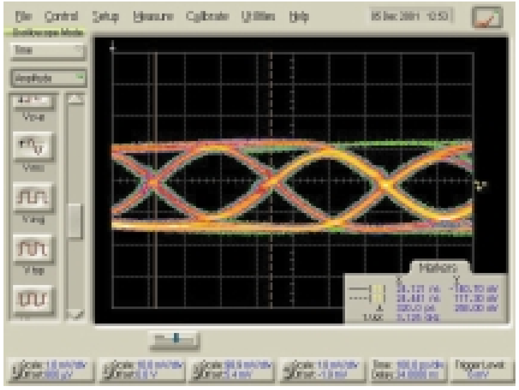


Figure 6: Receive eye after 40 inches of FR4 with 2 backplane connectors and 4 SMA connectors with pre-emphasis at 3.125 Gb/s

Note that the eye opening after 40 inches of backplane is 400 mV differential. With a receiver sensitivity of 60 mV, there is plenty of margin to provide unparalleled robustness. In summary, the Marvell 88X2040 product is a highly robust backplane SERDES solution that features the smallest package, lowest power and best signal integrity.

Following are the most significant advantages offered by the Alaska X SERDES device include:

1. Robust performance over 60 inches of FR4 traces
2. Lowest power
3. Smallest footprint
4. Compliance to IEEE 802.3ae
5. Flexible clocking
6. Superior jitter performance
7. Backward compatibility (lower data rates)
8. Latest process technology
9. Programmable amplitude and pre-emphasis

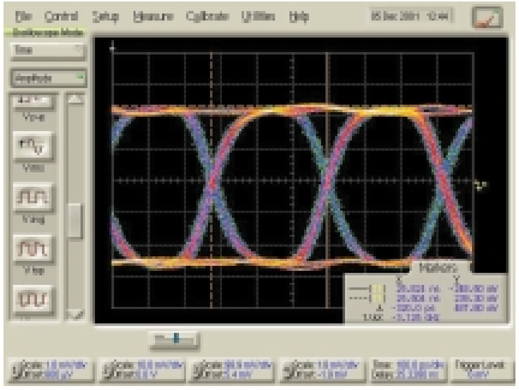
ASIC IP Cores

The Alaska™ X transceiver uses a 3.125 Gigabit Serializer/Deserializer (SERDES) IP core and input/output buffers such as high-speed 3.125 Gb/s drivers and HSTL buffers from the vast Marvell library of mixed-signal IP cores. Marvell has developed custom solutions leveraging such IP cores to build Application Specific Integrated Circuits (ASIC) with strategic partners. The Company's unique low power 3.125 Gigabit IP core is based on very high performance Phase Lock Loop (PLL) technology. The combination of low power dissipation, superior jitter performance and high noise immunity allows for the integration of large and complex system solutions on a single device. The Marvell Alaska X transceiver leverages four generations of SERDES technology from the industry-leading Alaska Gigabit PHY products, which are currently in high volume production.

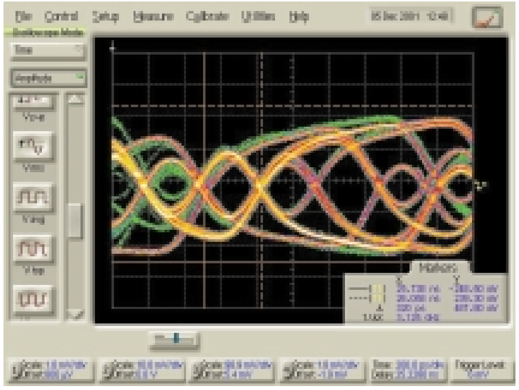
Side-by-Side Comparison of Transmit and Receive Waveforms at 3.125 Gb/s

WITHOUT PRE-EMPHASIS

Transmit

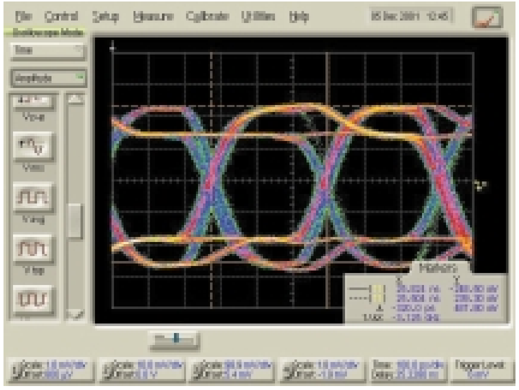


Receive after 40 inches

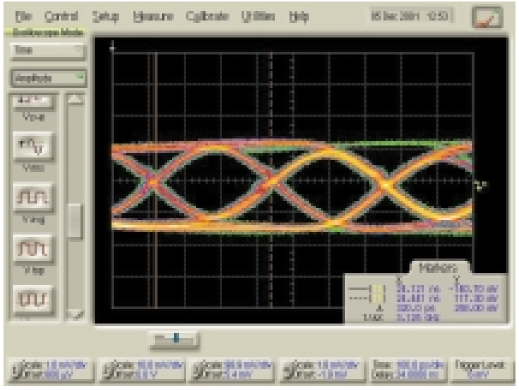


WITH PRE-EMPHASIS

Transmit



Receive after 40 inches



Scale: 200 mV/div (IEEE CRPAT)

References

[1] "XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)," IEEE Std. 802.3ae, draft 3.x.

[2] 10 Gigabit Ethernet Technology Overview White Paper. 10 Gigabit Ethernet Alliance http://www.10gea.org/10GEA_Whitepaper_0901.pdf.

[3] The Marvell Alaska X Transceiver Product information. http://www.marvell.com/Products/Doc_Files/2237/Alaska_X_Product_Brief.pdf.

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