Simple Techniques To Mitigate Tin Whiskers
On RoHS-Compliant Printed Circuit Assemblies
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Lead-free soldering technologies have increased electronics manufacturers' awareness of a metallurgical phenomenon referred to as whiskers. Whiskers occur most commonly in circuits where tin is used as a final finish on printed circuit boards (PCBs) and electronic components. In certain cases, microscopic single-crystal filaments (or hair-like protrusions) of the metal grow outward from the surface. Electrical system failures caused by short circuits between PCB traces or component leads are attributed to these growths.

Tin whiskers could be easily avoided by adding small amounts (as little as 3%) of lead to the plating. But since Europe's RoHS regulations required the elimination of lead from nearly all electronics products, there has been a renewed interest in the mechanisms causing whisker growth and how to control them. Many semiconductor companies, including STMicroelectronics (ST), have undertaken extensive programs to develop and certify processes that mitigate or eliminate whisker growth in most applications.

The first step was to investigate the phenomenon occurring on the tin plating. While not conclusive, studies show whisker growth is mainly due to internal compressive stresses near the metal surface. These stresses reach a critical level triggering the formation of whiskers, and are thought to be a way of reducing the system's internal energy. Internal stress in tin plated films may originate from a number of causes including organic contamination, atomic defects, and mismatches in the coefficients of thermal expansion (CTE) between the tin film and the base metal.

Early tin plating chemistries were designed to produce a shiny surface, known in the industry as bright tin plating. This is achieved by adding specialized chemicals to the plating bath that control the size of the grains and the planarity of the plated surface. Due to the properties of the metals and the high concentrations of additives required to achieve bright finishes, early bright tin plating techniques were prone to problems of organics co-deposition and atomic irregularities within the plated film. These irregularities, or alterations in the lattice spacing of the tin, are thought to have led to higher susceptibility of whisker formation.

One major change in some modern tin plating chemistries is the use of much lower levels of grain refining additives that produce a duller (or matte) appearance, and yet do not adversely affect its electrical properties. In a joint effort dubbed the E4 (Environmental 4) initiative, Infineon, Philips, Freescale and STMicroelectronics have identified a number of suitable commercial matte tin plating chemistries which are resistant to whisker growth.

Phase changes within the tin film can also cause localized compressive internal stresses. Since tin and copper normally form an intermetallic (Cu_6Sn_5) in a reaction that produces

a significant increase in volume, it is essential to take this into consideration for tin-plated copper lead frames or the net result of the combined penetration and expansion is a *wedge* driven into the tin layer at the grain boundary (see Fig. 1).

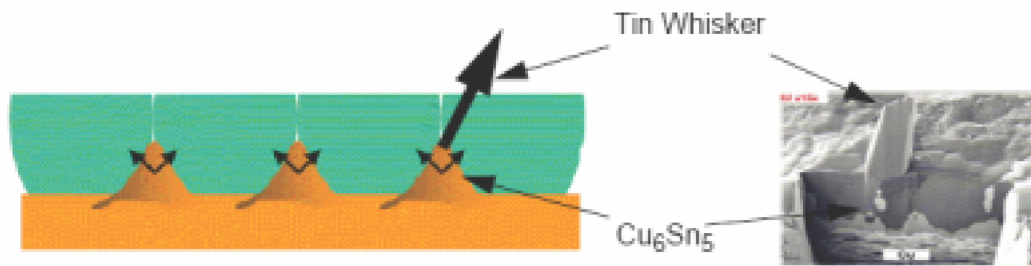

Fig. 1: Natural Growth Of Cu/Sn Intermetallic Compound At Room Temperature

Conversely, if the intermetallic is formed under higher temperature conditions (eg around 150°C), a different and more desirable intermetallic structure forms that is more uniform and contains practically no wedges (see Fig. 2). Using a 150°C bake to virtually eliminate the intermetallic wedges serves as the basis for the second component of the whisker mitigation strategy adopted by ST.

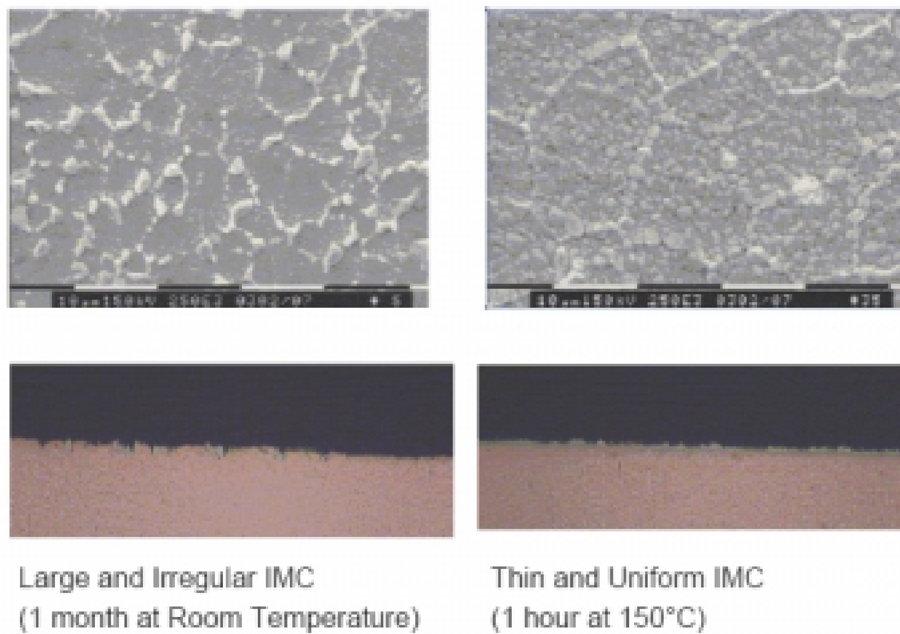

Fig. 2: Left: Intermetallic Allowed To Form At Room Temperature Over A Month; Large, Blocky, Irregular Cu6Sn5 Almost Exclusively At Grain Boundaries
Right: Intermetallic Formed By Baking Within 24 Hours Of Plating At 150°C; Very Uniform Layer Of Cu6Sn5 With Virtually No Wedges
(Extensive testing shows that, regardless of plating thickness, the whisker preventive effects of the 150•C bake extend past 400 days of storage at room temperature.)

Combining these two whisker mitigation techniques creates a coating that does not develop these whiskers, which can impact electrical performance or component reliability. A 400-day environmental test program that subjected about 1500 units from 40 different package types to a six-month ambient storage cycle, a six-month dry air storage cycle, plus 500 thermal cycles: (–35°C to +125°C) and a 500-hour exposure to temperature and humidity (85°C at 85%RH) produced no evidence of whiskers.

While much of this test plan was developed well before the March 1, 2006, release of JEDEC's JESD 201 *Methodology for the Assessment of Whisker Risk* and JESD 22A121 *Test Method for Whisker Growth*, this qualification plan satisfies more than 80% percent of ST customers. Nevertheless, ST will abide by this newer JEDEC standard and re-qualify the tin plating line in accordance with it.

Much of the research referenced in this TechNote is a result of the E4 initiative. Formed shortly after the European Union issued its RoHS directive, the group originally composed of three European semiconductor manufacturers (ST, Philips and Infineon) and grew with the addition of Freescale in 2003. E4's main focus is to study the phenomenon of tin whisker growth on packages and find ways to prevent this from posing a reliability hazard in the field.

References

1. Additional E4 (Environmental 4) initiative and research documentation can be found at http://www.st.com/stonline/leadfree/e3.htm.
2. Information on JEDEC's JESD 201 and 22A121 can be downloaded free from www.jedec.org (registration is required).

About The Author

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