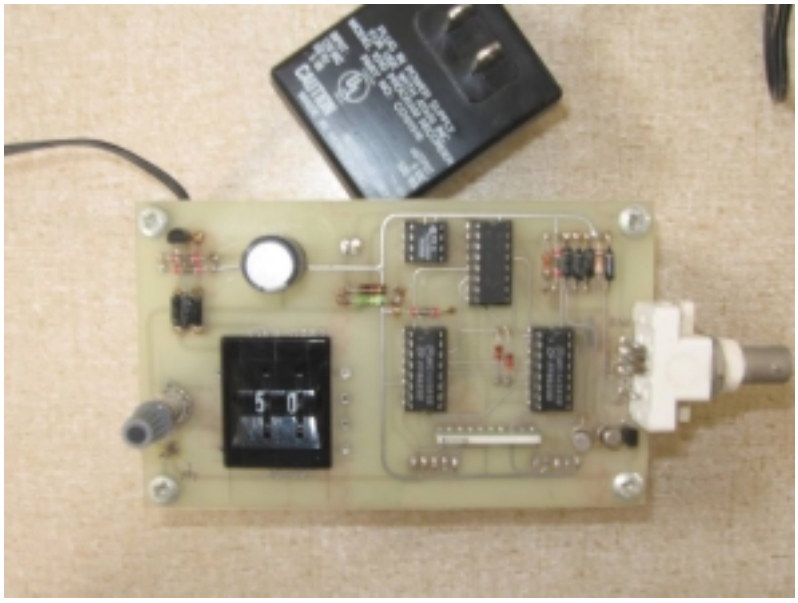
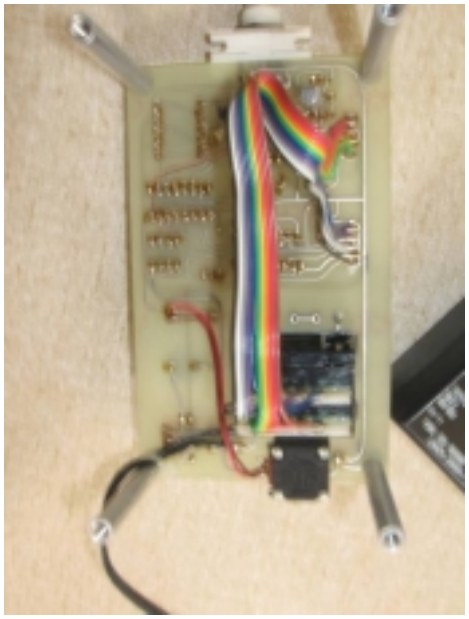
Build Your Own PWM Generator

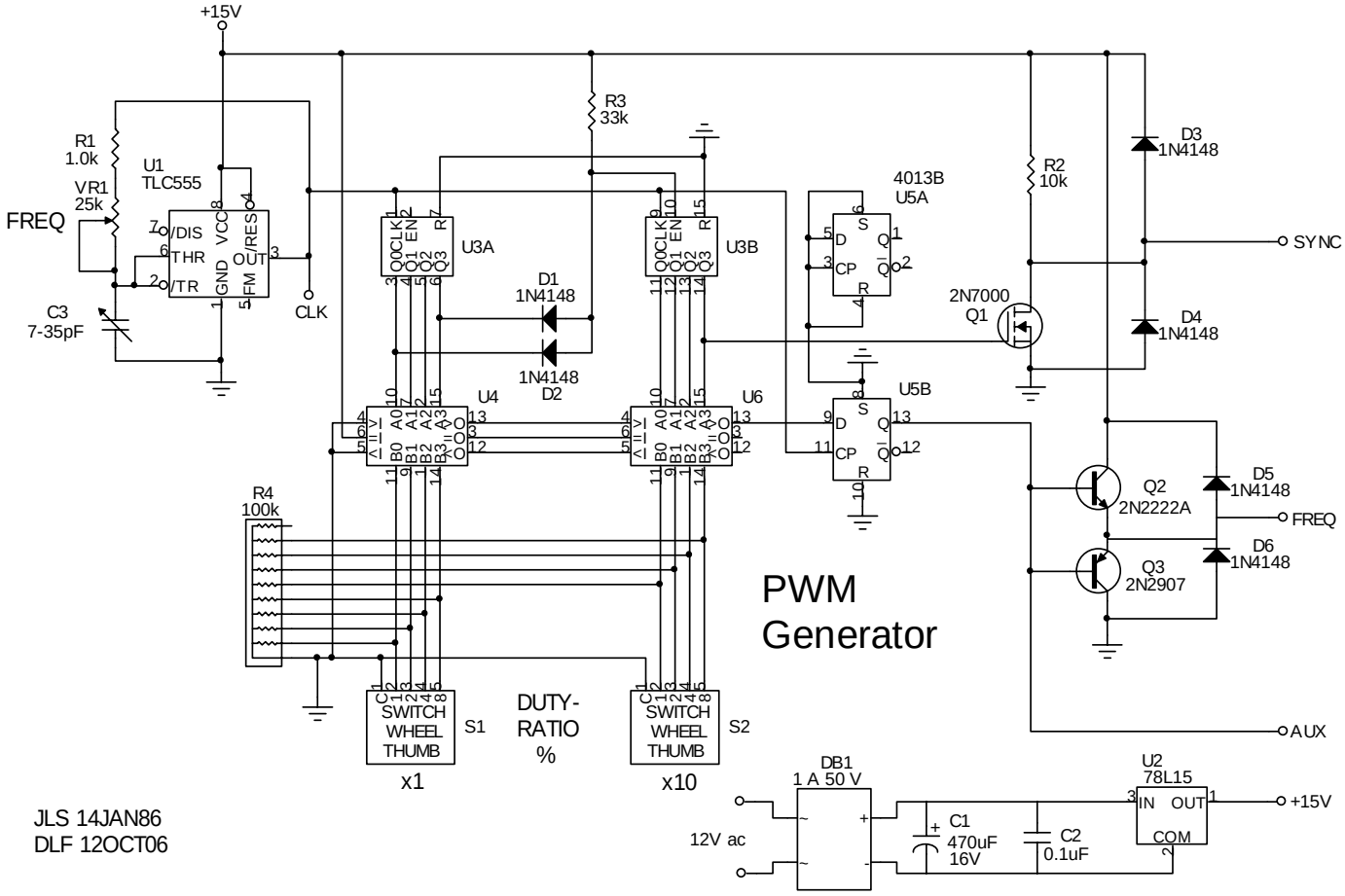
by Dennis L Feucht

In power electronics the need often arises to supply a square-wave with a manually-controlled frequency and duty ratio (duty cycle). With a few ICs, a two-digit thumbwheel switch, and glue parts, this simple bench instrument can be built and tested in an evening or two. The top and bottom views of a prototype are below.

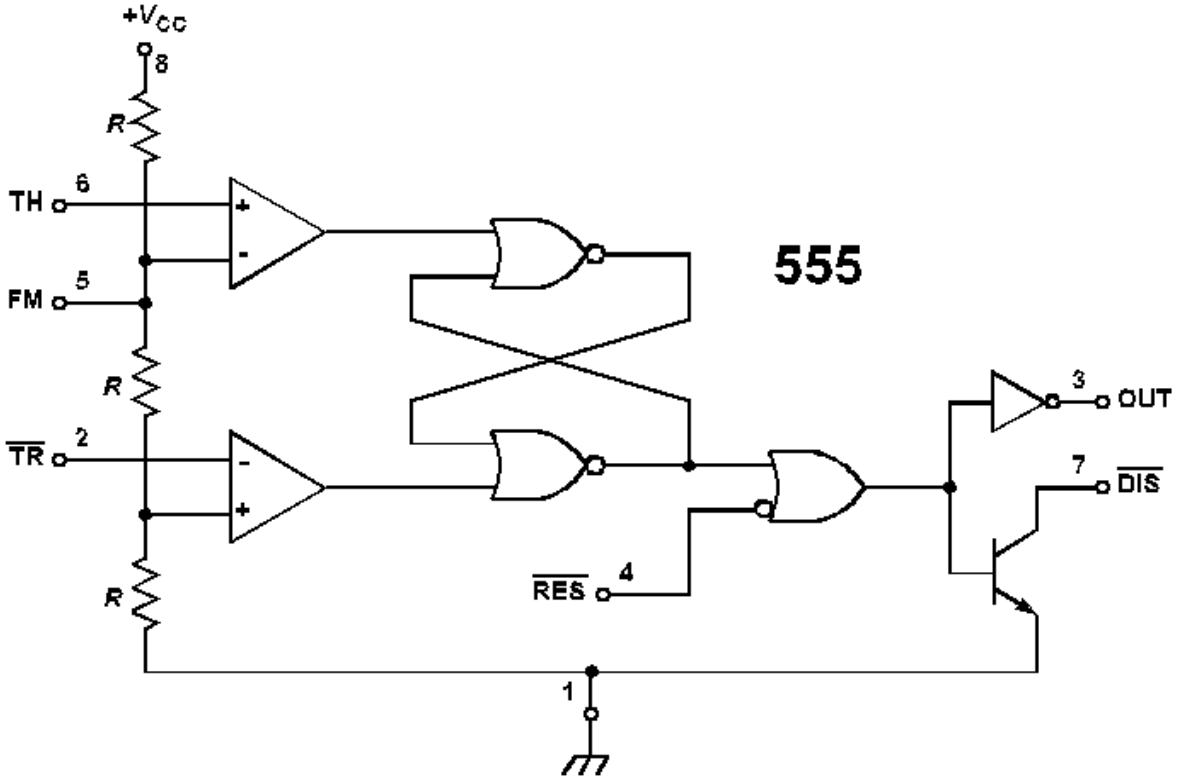




The circuit diagram of the PWM generator is shown below.



The CMOS 555 (which can be a TLC555 or a 7555) is the frequency generator IC. The variable resistance and capacitor set a time constant. The capacitor voltage increases exponentially from about 5 V (1/3 of the +15 V supply voltage), at which triggering occurs, to 10 V, the threshold (pin 6) comparator voltage, as set within the 555. The internal circuitry of the 555 is shown below.



In many timer applications where a 555 is used as a clock generator, the /DIS discharge output (pin 7) is connected through a series resistor to the capacitor. During the off-time of the output, this resistor discharges the timing capacitor, and allows independent control of the off-time. A very simple PWM generator could use this approach with a variable discharge resistance, though on- and off-times would be adjusted instead of the more convenient frequency and duty ratio.

In this application, the 555 is used to generate the frequency only, by running at a maximum frequency of 100 times the maximum PWM frequency. The CMOS logic 4518B is a dual decade counter. It divides the clock frequency by 100 and its outputs are compared to two decade thumbwheel switches. When the 4518 count equals or exceeds the thumbwheel value, the cascaded 4585B comparator output changes and is synchronized to the clock by the 4013 D flip-flop. This avoids glitches (*runt* pulses) at the output, resulting in a clean PWM waveform.

The overflow of the counter marks the boundary of a cycle and is buffered by the 2N7000 MOSFET as a SYNC output for oscilloscope external triggering. For direct drive of power MOSFET gates, the D-flop output is also buffered, with complementary BJTs, as the FREQ output. The unbuffered waveform is also provided for triggering and diagnosis as an AUXiliary output. Protection diodes are placed on the SYNC and FREQ outputs. The +15 V output provides plenty of gate drive voltage for power MOSFETs.

Having a PWM generator at all is sometimes sufficient, and is preferred to not having a fancy one. This design offers such an option, especially for those eager to get on with their bench work. This simple PWM generator can easily be improved in many ways. A simple one would be to use the second half of the D flop as a complementary output, with BJT buffering, so that both the duty ratio, D, and its complement, $D' = 1 - D$ are simultaneously available as outputs.

I have a few remaining protoboards of the above generator. The 4013 was not included in the layout and must be added by flipping the part, gluing it to the backside of the board, and adding a few wires. If you are interested in obtaining an unpopulated board, please contact me through http://www.analogzone.com. If the response is large enough, it might merit a new board iteration -- perhaps with some enhancements.