

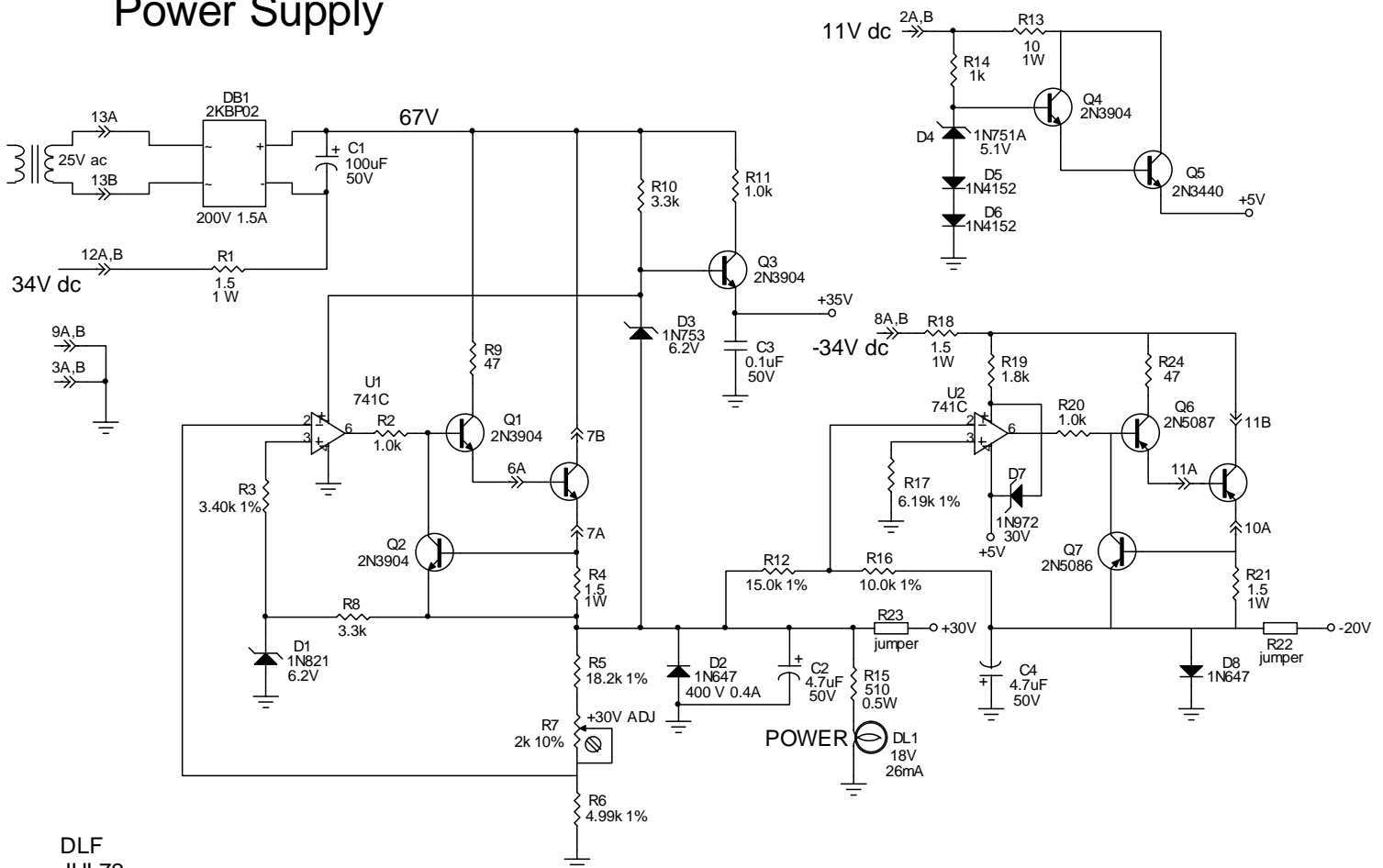
Build Your Own Sweeping Function Generator Power Supply, Output Amplifier, and V/I Converter Circuits

by Dennis L Feucht

The FG506 sweeping function generator circuit design took place in the summer of 1973. Consequently, the level of integration is at most MSI (for the digital logic). A positive consequence is that no parts are mysteriously customized and undocumented. The board is two-layer through-hole, and the design could easily be simplified by being upgraded to use present-day ICs. (That might be a follow-on project.) The original, known-good design will be retained here, with comments given on upgrading. A '70s design also provides educational value for circuit-level understanding of analog electronics.

Power Supply

Power Supply



DLF
JUL72
redrawn 30MAY06

The necessary, but least interesting, subsystem of the FG506 is the power supply, shown above. It is chosen to be first because it provides a context for the FG506, which is a Tektronix TM500 plug-in instrument. The use of plug-ins made oscilloscopes more versatile, and the idea was extended to instruments in general. Instead of having redundant power supplies, power cords, and boxes, one mainframe could hold several instruments which shared a common infrastructure. A TM500 mainframe contains a power transformer and heat-sunk power transistors for linear power supplies, which were in common use in the '70s. This kept heat out of the plug-ins. (Nowadays instead, our desks are cluttered with little switching-supply boxes -- hardly an

improvement in packaging!) The TM500 mainframe was a somewhat strange subsystem. Each plug-in connector had plenty of extra pins beyond those needed for power supply functions for connections between instruments. Yet no grand, elegant plan for interconnection ever arose. Different instruments run various signals to pins on the motherboard connector in the rear, and these are shown on the FG506 schematic diagrams with their rear-connector pin numbers.

Another non-intuitive aspect of the TM500 was the choice of power supply voltages. In the FG506, there are +35 V, +30 V, +20 V, +5 V, and -20 V supplies, hardly voltages one would be inclined to use nowadays. (With a little work, the FG506 design could be scaled for computer supply voltages.) Consequently, power dissipation is large relative to today's power-conscious designs. The number of different supply voltages is also rather non-minimalist too.

The mainframe has unregulated ± 34 V and +11 V supplies and, along with a 25 Vrms ac winding, were used to derive all the supply voltages using zener-diode or op amp-based feedback circuits for regulation. Jumpers R22, R23 are not necessary but they make power-supply problems easier to diagnose when a supply output needs to be disconnected from its load. D1 is the voltage reference for the +30 V supply. (Why is R3 1%? I don't have a clue other than that I designed this instrument when I was 22 years old. Perhaps it is to match its TC to that of R5, R6 for op amp input current compensation.) When the feedback divider is included in the output-voltage calculation, and the trim-pot is centered, the voltage turns out to be:

$$V_o = (6.2 \text{ V}) \cdot \left(\frac{18.2 \text{ k}\Omega + 2 \text{ k}\Omega + 4.99 \text{ k}\Omega}{1 \text{ k}\Omega + 4.99 \text{ k}\Omega} \right) = 26.0 \text{ V}$$

With the trim-pot at the high-output extreme, the output calculates to be 31.3 V. Obviously, the divider values could be better chosen to center the adjustment, such as a choice of 23.2 k Ω , 1 % for R5. R7, a cermet trim-pot, is kept relatively small in value to minimize the effect of its larger TC than that of R5, R6. Q2 provides simple current-limiting overcurrent protection. Q1, a 2N3904, might better be a 2N2222A (or a PN2222 nowadays) because it is designed for a peak β at higher currents than the 2N3904, which peaks at about 7 mA. (I would reduce the number of different BJT types in the FG506 design by using (for npn) PN3904 and PN2222 and (for pnp) PN3906 and PN2907 nearly everywhere they can be applied. The latter pair are for higher currents in the small 100s of mA.

The +35 V supply stacks onto the +30 V supply using a Zener diode translator, up to the immense 67 V unregulated supply. (This scheme is not power-efficient!) Likewise Q1, Q3 might well be a PN2222 also -- and Q4. Q6 might be a PN2907.

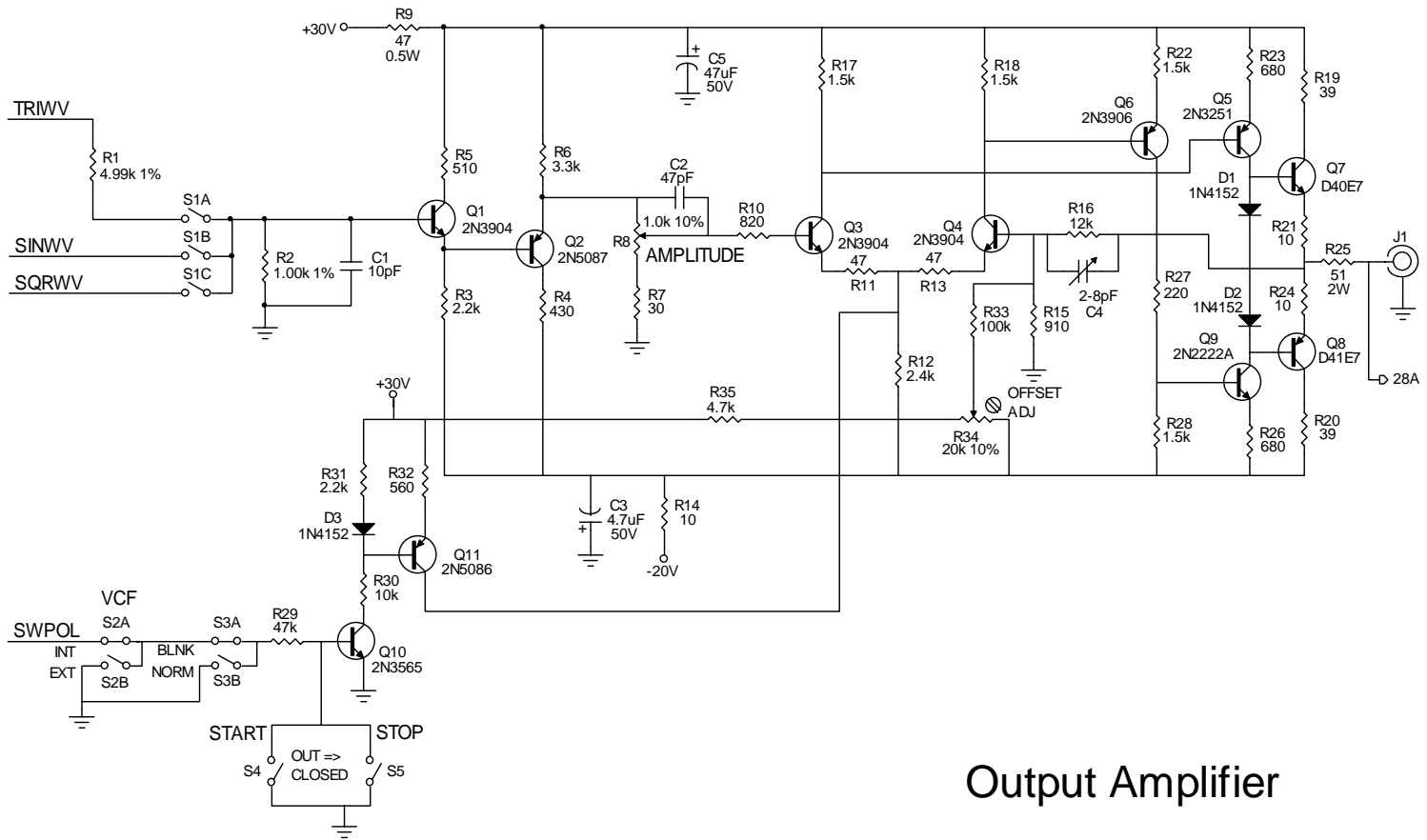
The -20 V supply feedback divider does not need adjustment for around 2% accuracy if the +30 V supply is well-adjusted, for the -20 V supply uses the +30 V supply as a reference. Q7 is another overcurrent protection circuit. D2 and D8 keep the outputs from being reversed in polarity if something bad happens. The front-panel power indicator, DL1, an incandescent, is quickly replaced by an LED and R15 made a 10 k Ω , 0.25 W resistor. Like R3, R17 need not be 1%. R3 can better be 3.9 k Ω , 5 % and R17 6.2 k Ω , 5 %. D2 and D6 might each better be 1N4002.

Output Amplifier

Shown below is the output amplifier. The input is selected from triangle, sine, or square waveforms. The output, at J1, is intended to be able to drive a terminated 50 Ω cable.

Q1 and Q2 provide $\times 1$ buffering to the amplitude control. Its output drives the input of a power feedback amplifier used in the noninverting configuration. The diff-amp input stage (Q3, Q4) drives a complementary

(pnp) common-emitter (CE) stage (Q5, Q9). However, the negative-side driver requires an extra stage of inversion, provided by Q6. It has a gain of about -1, to keep the loop gain of the positive and negative paths about the same, for their dynamic response to be similar. The loop gain is realized in the first two stages; the Q6 inverter and Q7, Q8 CC (emitter-follower) output stages have essentially a $\times 1$ magnitude of voltage gain.



Output Amplifier

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The diff-amp stage has a standing current in the two transistors of about $19.2 \text{ V} / 2.4 \text{ k}\Omega \cong 8 \text{ mA}$, or 4 mA per transistor. Then $r_e \cong 26 \text{ mV} / 4 \text{ mA} = 6.5 \Omega$. The base resistance is about $1 \text{ k}\Omega$, and when referred to the emitter circuit with a β of 200 adds another 5Ω per side. Then the one-sided emitter-circuit transresistance is approximately:

$$r_M \cong R_B / (\beta + 1) + r_e + R_E \cong 5 \Omega + 6.5 \Omega + 47 \Omega \cong 60 \Omega$$

At the output, the load resistor of $1.5 \text{ k}\Omega$ is shunted by the input resistance of the next stage, which is about $(\beta + 1) \cdot (680 \Omega)$. This reduces the load resistor values by less than 2% -- a negligible amount for these approximate calculations. Then the differential stage gain is:

$$A_{v1} \cong \left(\frac{R_L}{r_M} \right) = 25$$

The gain of the CE (Q5, Q9) stage is also of the form for A_{v1} , but R_L in this case varies significantly with amplifier output resistance. Unloaded, it can be high, but with a $50\ \Omega$ load, per each side, $R_L \cong (200) \cdot (110\ \Omega) = 22\ \text{k}\Omega$. Then the voltage gain is:

$$A_{v2} \cong 2 \cdot \left(\frac{22\text{k}\Omega}{680\ \Omega} \right) \cong 65$$

The forward-path voltage gain is consequently about 1625. The feedback path is the divider with attenuation of:

$$-H = \left(\frac{910\ \Omega}{12\ \text{k}\Omega + 910\ \Omega} \right) = 70.5 \times 10^{-3} = 1/14.2$$

Then the feedback loop gain is about 114, just enough to keep gain error within what the spec requires. When the amplifier is unloaded, the loop gain will be higher and the response correspondingly less damped. The stability margin is less under that condition.

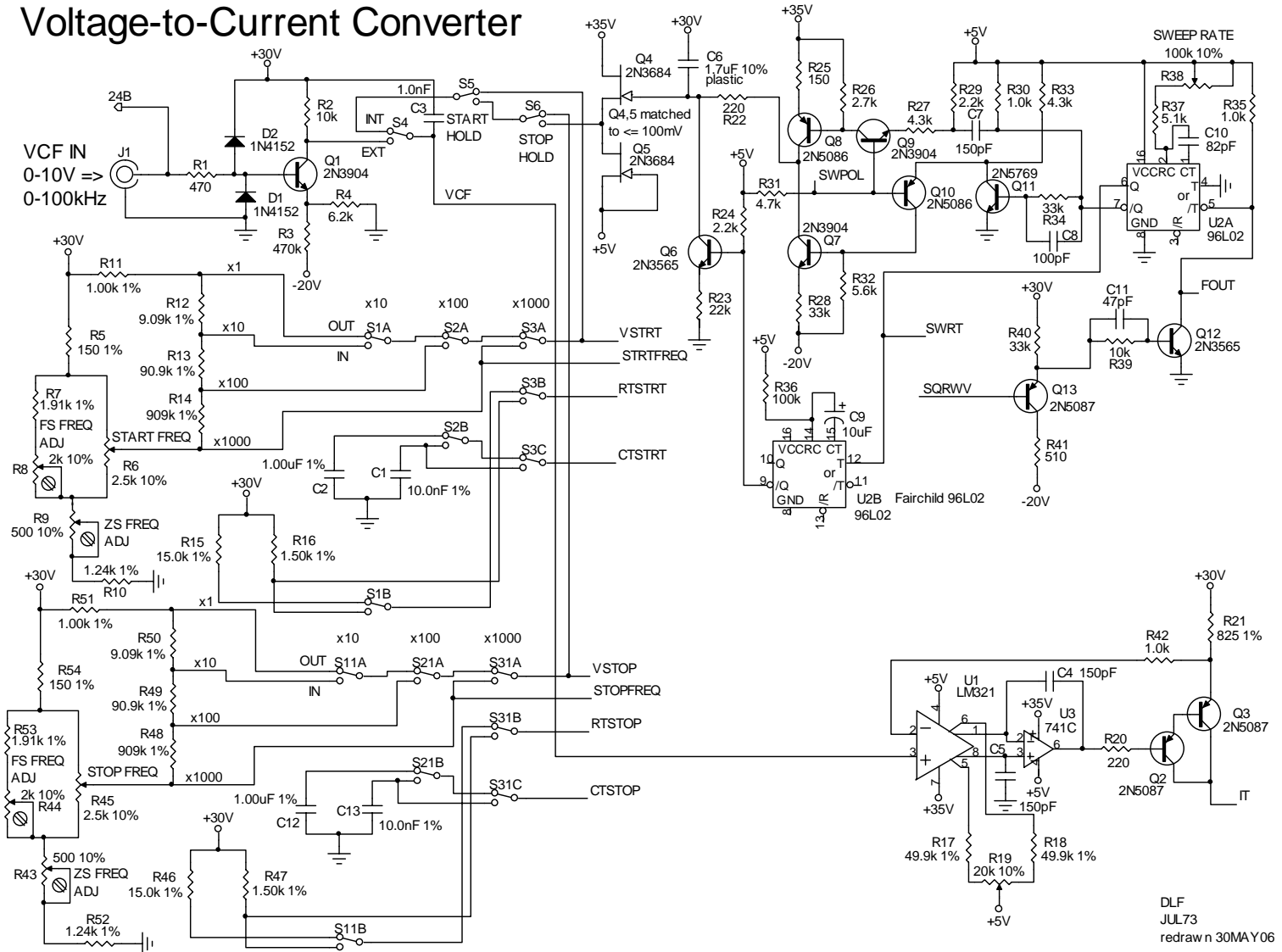
One additional feature of the output amplifier is the connection of Q11 to the diff-amp emitter circuit. This is used to turn off the amplifier (0 V drive out) when the blanking button is asserted on the front-panel. The output can thus be blanked during the down sweep or frequency retrace. SWPOL is a logic high during the down sweep, causing Q10 and Q11 to be on. Q11 collector current causes the diff-amp BJTs (Q3, Q4) to be off and the succeeding stages remain undriven.

Blanking is defeated if the START or STOP FREQ buttons on the frequency dials are set to the out position. No blanking occurs either when the VCF source is EXTERNAL (S2A) or if the blanking is off (S3A) in the NORMAL position.

Voltage-To-Current Converter

The FG frequency is set by the timing current supplied to the generator loop. More significantly, timing currents are generated for precise-duration pulse generation by two discrete MMVs, used to detect the end (start and stop) frequencies. Control of the sweep rate and the generation of the exponential VCF (for log sweep on a display) are included in the circuit diagram, shown below.

Voltage-to-Current Converter



In the lower right corner, IT, the timing current is output from Q2, Q3. Along with U1, U3 and associated components, they form a precision voltage-to-current (V/I) converter. Because of the lack of precision monolithic op amps in the early 70s, a precision preamp, the LM321, was used to drive U3, with input offset trim (R19). The input voltage to the LM321 is the frequency-controlling voltage (VCF).

When the VCF is derived from an external source (through J1 or pin 24B on the plug-in rear connector), Q1 scales it to match the VCF voltage range. R1, D1, and D2 provide input protection for Q1. At its collector, the VCF range is about 15 V for a 10 V input.

When the start or stop hold buttons are asserted, VCF is set by VSTART or VSTOP, filtered by C3. These voltages are derived from the dividers and front-panel range switches shown on the lower left. Four frequency ranges are provided, and the zs and fs calibration of the frequency dividers is achieved using two

trim-pots on each divider. The range switches also select between two timing resistors and two timing capacitors for the start and stop MMVs (to be discussed later). This gives four combinations and hence four decade ranges for the MMV pulse durations.

The triangle-wave generator also generates square-waves, at node SQRWV. This waveform is processed by Q13, Q12 and output in TTL-compatible form as FOUT. It is used to trigger MMV U2A. For each cycle of the output waveform, U2A outputs a pulse, SWRT, of a duration set by the SWEEP RATE front-panel pot. It triggers the other half of the dual retriggerable MMV, U2B, keeping it set (Q high) unless the generated frequency decreases to below the timeout of U2B, less than the 10 Hz minimum FG frequency. This MMV is used to cause recovery of VCF in case the sweep frequency undershoots to zero. Without an input trigger to U2A, no decrement in VCF occurs and sweep-current integrating capacitor, C6, remains discharged at 0 V. This lock-up condition is overcome when U2B times out and turns on Q6, which supplies current to C3 and VCF becomes non-zero. Then IT becomes non-zero and the generator loop begins to run again.

The other path from /Q of U2A turns off Q11 for a specified duration, allowing Q10 to conduct R33 current, if SWPOL is low (up sweep). This causes Q7 to conduct, charging C6. The C6 voltage is buffered by Q4, Q5 and output as VCF to the V/I converter.

When SWPOL is high (down sweep), Q10 is kept off. The U2A /Q output is differentiated by C7, R29 and its pulse of current, independent of the U2A duration, is delivered through Q9, causing Q8 to conduct and discharge C6. Consequently, the down-sweep rate occurs at a fixed rate, though it is still exponentially decreasing as output frequency decreases. When SWPOL is low (up sweep), Q9 is disabled.

In the next part, the remaining circuitry will be explained: the generator loop, frequency control, and sine converter.

