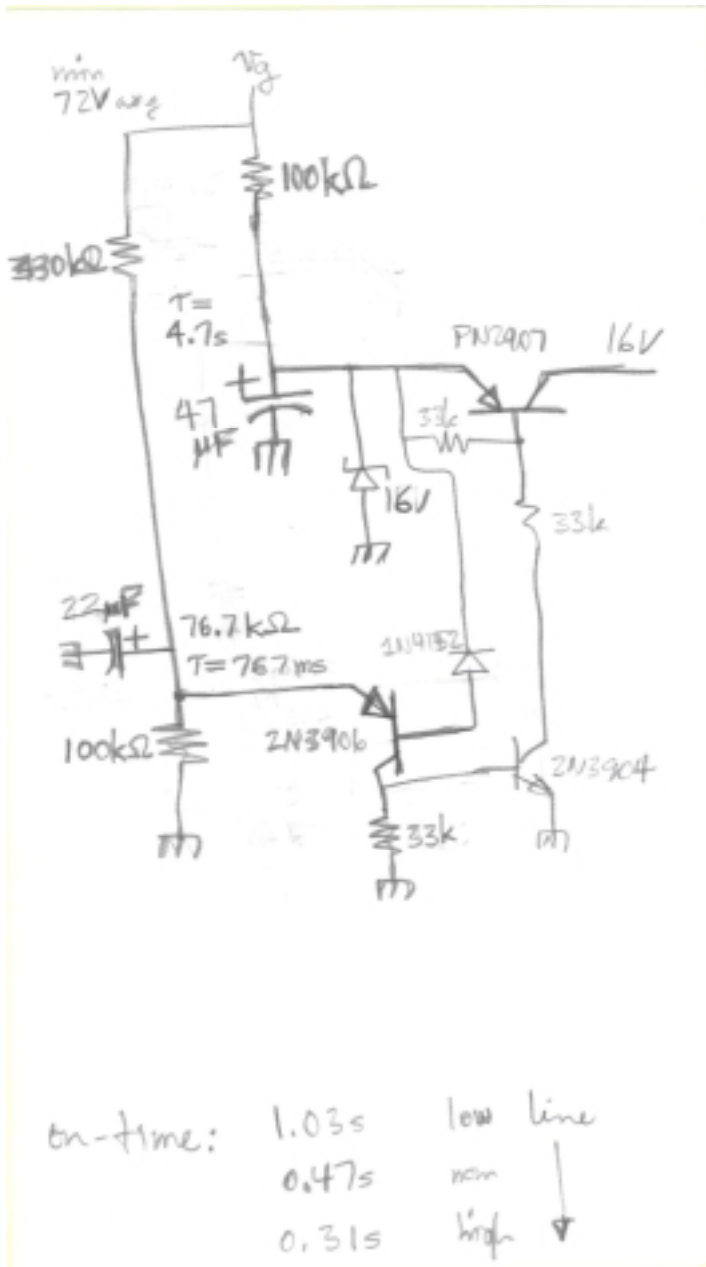


Power Converter Power Supply Design Problems
 by Dennis L Feucht

Q: I am designing a cost-sensitive off-line power converter with a PFC input stage that also needs to dissipate low standing power -- that is, the power used by the PFC itself must be kept minimal. I need to power the control circuitry on the primary side of the converter, and if I use a resistive divider down from the unregulated supply, it will dissipate too much power. Any recommendations on a lower-power circuit?

A: This problem can be solved by using two different schemes to power the control circuitry. The first derives power in the manner you describe above, through a dc connection to the unregulated supply. However, once start-up occurs, a separate supply provides power much more efficiently. The start-up supply then must somehow be turned off without causing a discontinuity in power to the control circuits.



To illustrate some ways this design problem can be solved, consider the discrete BJT start-up circuit shown here as scanned from a project notebook page. The supply voltage, v_g , is derived from the rectified power line and its average voltage (being a rectified sine wave) at low line is 72 V. The start-up supply provides 16 V to the control circuitry.

A divider from v_g consisting of 330 k Ω and 100 k Ω resistors drives the emitter of the 2N3906 pnp BJT. The emitter node also has a 22 μ F C to ground, forming a time constant of 767 ms with the 76.7 k Ω resistance at that node.

A 100 k Ω resistor from v_g drives the emitter of the PN2907 pnp pass BJT, a 16 V Zener diode and a 47 μ F capacitor to ground. The time constant is much longer than the other, at 4.7 s. The PN2907 BJT has a 33 k Ω base-emitter resistance which will keep it off if base current is not supplied.

The sequence of events is as follows. At power-on, v_g increases to at least 72 V average. The 2N3906 emitter node rises more quickly than the PN2907 emitter. While the PN2907 emitter node voltage is less than the 2N3906 emitter, the 2N3906 base diode will be forward biased and it will conduct, turning on the 2N3904 and consequently, the PN2907. The “16 V” output will follow the PN2907 emitter voltage.

Although the RC circuit of the PN2907 emitter is slower in rising, it has v_g as a target voltage,

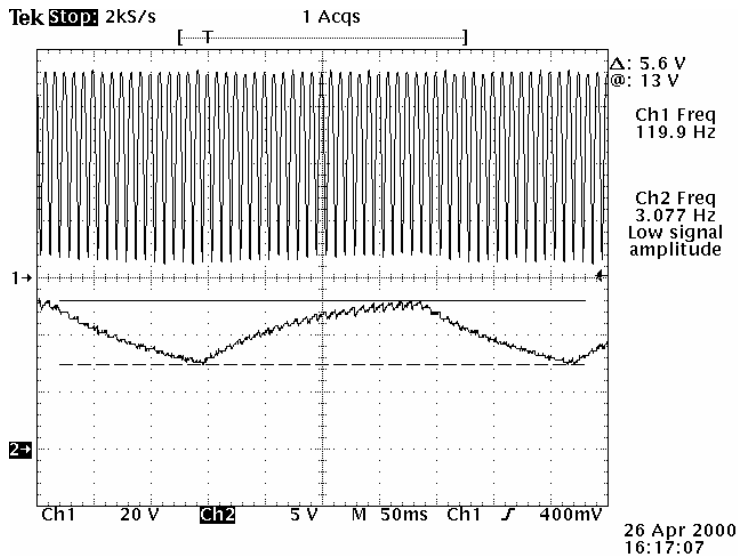
whereas the RC of the 2N3906 emitter has $v_g/4.3$ instead. For the minimum average line voltage, this target voltage is only 16.7 V, not quite enough to keep the 2N3906 on. As the average v_g rises, the 2N3906 emitter voltage settles to this asymptotic value while the PN2907 emitter continues to rise until clamped by the 16 V Zener diode. At this voltage, the 2N3906 no longer has enough forward voltage across its $b-e$ junction and it turns off.

The brief time in which the 16 V supply is on varies with line voltage. According to measurements, it is longest (1.03 s) at low line, 0.47 s at mid-line, and 0.31 s at high line. The decrease in on-time with V_g is expected because the PN2907 emitter voltage reaches 16 V sooner relative to the exponentially rising voltage at the 2N3906 emitter.

Start-Up Problems

Some of the common problems with start-up circuits are:

1. v_g stays low too long, causing excessive i_g which blows the fuse
2. The control IC turns on, loading the start-up supply excessively before the bootstrap supply can provide adequate power. Start-up voltage decreases under the additional load until the IC turn-off threshold is crossed. The control supply voltage then oscillates between the turn-on and turn-off voltage thresholds, as shown below.

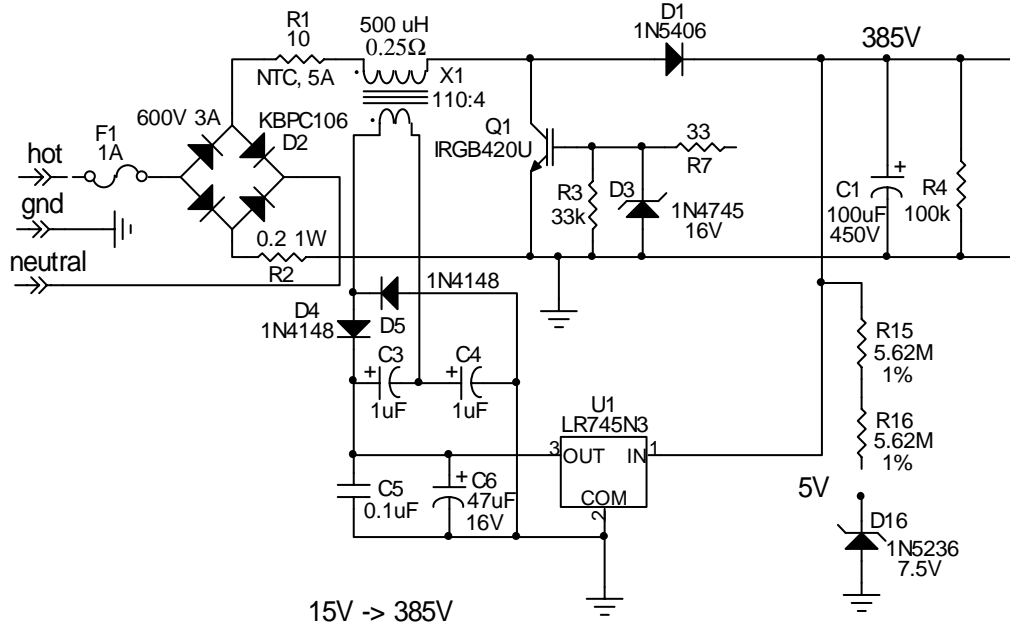


3. Large compensation capacitors in the feedback loop (such as around the error amplifier) charge adequately to allow the high duty-ratio needed at start-up (due to low v_g), and the bootstrap supply fails to deliver adequate current to drive the IC
4. Power-factor correction (PFC) circuits have a rectified sine input and this can cause additional complications, especially when there is a switching waveform superimposed upon the $|\sin|$ -wave

We will now look at some start-up circuits that (usually) avoid these problems.

The circuit shown below has undervoltage (UV) disabling (or lockout). As C1 charges through R2, R8, the Zener D1, Q2, and Q1 remain off until the C1 voltage exceeds 16 V. D1 then conducts, forward-biasing Q2 which then turns on Q1. While this circuit supplies about 16 V out, it has no turn-off mechanism as shown. One scheme that was tried was to precede it with a three-terminal Supertex LR745N3, itself a start-up circuit without undervoltage disabling. Its output rises at power-on until it reaches about 21.5 V. With a PFC input, it could drop down below 13.25 V. When this happens, the output is turned off until it falls below 7 V, whereupon it turns back on. (This behavior led to the oscillating phenomenon in the previous oscillograph.) (For non-PFC applications, the LR745 worked as required.)

Another scheme is shown below, used on a PFC boost converter. The boost inductor was a low-cost type, wound on a ferrite rod. I modified the inductor by adding a couple of layers of the usual (yellow, for some reason) polyester tape used to isolate transductor windings. Then I wound the calculated (few) turns of small-sized wire around it, as the following circuit diagram shows.



A photo of the prototyped test circuit is shown below.



This circuit is not expensive, including the additional labor in adding the winding to the inductor, has few parts, yet works well. I recommend adding it to your circuits repertoire.

