

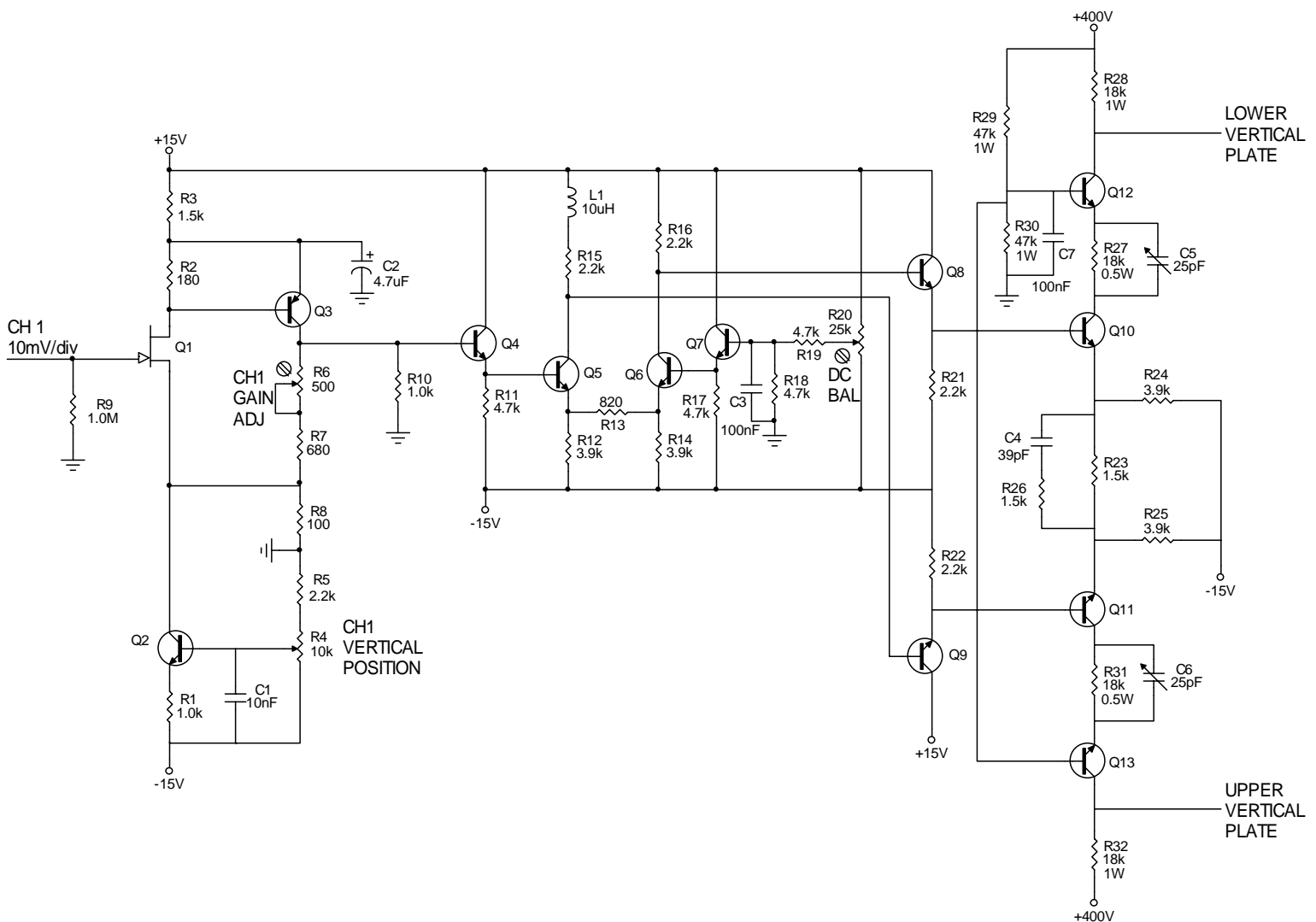
What's Wrong With This Circuit?

by Dennis L Feucht

This circuit design clinic is reminiscent of those visual amusements for children asking them "What's wrong with this picture?" The exercise is to find as many errors as possible, in this case, of a given circuit design.

Instead of subjecting the circuits of others to critique, or even ridicule, the following circuit diagram is most of the vertical amplifier of the first oscilloscope I ever designed (in my late teens) for my own use. As an amplifier, this circuit exercise applies to a wide range of analog circuit applications, not only to 'scopes. I needed a calibrated 'scope for my home laboratory, and got a good deal on a used Knight-kit oscilloscope, which gave me the chassis, power supply (especially the CRT high-voltage supply), CRT circuit, and front-panel. I gutted the rest and redesigned what became my first *laboratory-quality* oscilloscope.

Needless to say (as you will see), my design skills were in their early developmental stage, and this design provides plenty of opportunity to find various errors in the form of suboptimal design decisions. Find as many as you can without changing the basic circuit topology. R9 is the simplification of the preceding input attenuator. (For "design-grade" attenuator concepts, see the book put out by Springer titled *Wideband Amplifiers* by Peter Staric and Erik Margan.) With its commonly-used circuit stages, the design has enough basic faults to provide skill enhancement to a wide variety of readers. See how many you can find.



Circuit Design Review

Some preliminary comments on what the amplifier is might help to put the error list in context. The first stage is a JFET-input feedback amplifier consisting of Q1 - Q3. Q2 provides static (bias) current for Q1 and the amplifier static (dc) output voltage can be varied by changing this current with the vertical position control.

Q4 is an emitter follower that provides inter-stage buffering. It drives the differential amplifier stage, Q5 - Q7. The differential outputs of Q5, Q6 drive another stage of buffers (Q8, Q9) which in turn drive the cascode output stage, Q10 - Q13. Q7 compensates for the *b-e* junction of Q4 and provides Q6 base voltage. It can be adjusted to achieve differential amplifier balance -- that is, to remove static voltage offset from the diff-amp.

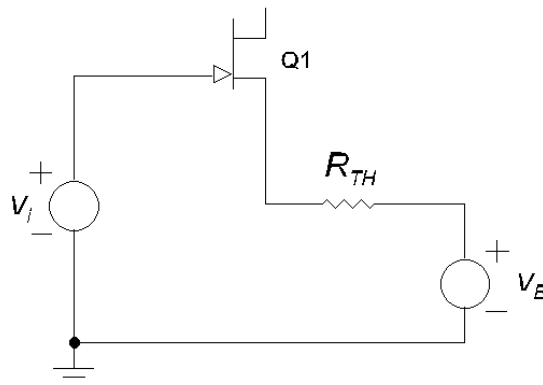
The differential cascode deflection plate driver has a high-voltage output, to bias the vertical plates at the correct static (quiescent) voltage for correct CRT operation. The CRT has an electric field, E , across its length, from electron gun at the cathode to high-voltage phosphor screen. The voltage gradient due to this field, $E \cdot l$ (where l is length), is consequently increasing with l from cathode to plate. Depending on the location, the field will correspond to a certain voltage. The plates are consequently specified to have a given static voltage corresponding to this field-produced voltage at their location within the CRT so as not to disturb the electron-beam optics. The deflection plate sensitivity (in V/div, where "div" is a major graticule division on the screen) can be calculated based on the 10 mV/div sensitivity at the input and the overall amplifier voltage gain.

Assuming the adjustment pots are designed for nominal center values, and that the transistors have β of a typical 199 ($\beta + 1 = 200$), then the centered Q2 collector current is:

$$\frac{\frac{5 \text{ k}\Omega}{2.2 \text{ k}\Omega + 10 \text{ k}\Omega} \cdot (15 \text{ V}) - 0.75 \text{ V}}{1.0 \text{ k}\Omega} \cdot \frac{199}{200} \cong 5.37 \text{ mA}$$

Assuming that the $I_{DSS}(Q1)$ is near this value of current, and that the JFET transresistance, $r_m (= 1/g_m) = 200 \text{ }\Omega$, then the open-loop gain of the amplifier can be calculated.

In analyzing the feedback loop, the output quantity, the voltage at the collector of Q3, is also the feedback quantity. Second, we must choose the feedback error quantity. $v_{GS}(Q1)$ is one choice, where v_S is the feedback summing quantity v_B , (the output of feedback network H , in control language). The choice of v_B for this analysis is the Thévenin equivalent voltage of H , as shown below.



In this circuit, the input voltage feedback summing loop subtracts v_B from v_i across a resistance of $r_m(Q1)$ in series with R_{TH} , the Thévenin resistance of the feedback divider consisting of $R_f = R6/2 + R7$ and $R_i = R8$.

Then Thévenizing:

$$R_{TH} = \frac{R_f \cdot R_i}{R_f + R_i}$$

and:

$$v_{TH} = v_B = \left(\frac{R_i}{R_f + R_i} \right) \cdot v_o$$

The assumption at the output node is that v_o is the actual (loaded) circuit voltage. This means that when calculating the forward-path gain, G , that the loading of the next stage, including R10, and that of the H divider be included.

Now that the error quantity, v_E , has been chosen to be across $r_m + R_{TH} = r_M(Q1) = r_{M1}$, then the forward-path quasistatic (low-frequency) incremental (small-signal) voltage gain is:

$$G = \frac{v_o}{v_E} = \left(-\frac{R_2 \parallel r_{e3}}{r_{m1} + R_{TH}} \right) \cdot \left(-\frac{(R_f + R_i) \parallel R_o}{r_{e3}} \right)$$

This assumes that C2 is chosen to be large enough for the emitter of Q3 to be a dynamic (ac) ground. At some low frequency, it is not, and the break frequency must be accounted for in $G(s)$, but that will not be done here; R2 will be taken as the load resistance and R3 is for biasing only.

Additionally, R_o is the next-stage loading on the feedback stage. It is affected by R10 and Q4 - Q7, reaching as far as R20. Applying the β transform, the exact (BJT T-model) expression is:

$$R_o = R_{10} \parallel (\beta_4 + 1) \cdot (r_{e4} + (R_{11} \parallel (\beta_5 + 1) \cdot (r_{e5} + (R_{12} \parallel R_{13} + (R_{14} \parallel (r_{e6} + \frac{R_{17} \parallel r_{e7} + (R_{18} \parallel (R_{19} + R_{20} / 2) / (\beta_7 + 1))}{\beta_6 + 1}))))))$$

Plugging in resistor and β values, $R_o \cong R_{10} = 1.0 \text{ k}\Omega$ for $\beta \gg 1$. Then to calculate the gain of Q3, r_{e3} must be known and it depends on I_{E3} . If the loop has high gain, then for zero V_I , V_O will also be zero, the gain having driven the error to near-zero. This implies that I_{E3} must also be near-zero. Some V_{GS} at zero will allow for non-zero I_{E3} , which will vary greatly with V_I . Open-loop gain depends greatly upon static currents which depend greatly upon input or output voltage.

Assuming that the loop gain is sufficiently high (for r_{e3} sufficiently low), then $v_B \cong v_i$ and closed-loop voltage gain becomes:

$$A_{v1} = \frac{v_o}{v_i} = \frac{R_f}{R_i} + 1 = \frac{250 \Omega + 680 \Omega}{100 \Omega} + 1 = 10.3$$

The Q5 side is CE while Q6 is CB. The CE will be degraded in bandwidth by the Miller Effect and is consequently compensated using series inductive peaking, with L1.

The first-stage output is buffered by a CC stage, which can be considered the symmetrical counterpart of Q7. This diff-amp generates the differential output across the collectors of Q5, Q6. The gain, calculated using the transresistance method, is:

$$A_{v2} = \frac{v_{o2+} - v_{o2-}}{v_{i2}} \cong 2 \cdot \frac{R_L}{r_e + R_E / 2} = 2 \cdot \frac{2.2 \text{ k}\Omega}{7.5 \Omega + 820 \Omega / 2} = 10.5$$

The single-ended gains, $v_{o2\pm}/v_i$ are half A_{v2} . Following the second stage are CC stages, which reduce inter-stage loading. They also reduce voltage gain by a few percent.

The output stage is a differential cascode with CB BJT's biased at half the supply voltage, or 200 V. The voltage gain is:

$$A_{v3} = \frac{v_{o3+} - v_{o3-}}{v_{i3+} - v_{i3-}} = \frac{R_L}{r_e(\text{CE}) + R_E/2} = \frac{18 \text{ k}\Omega}{7.5 \Omega + 1.5 \text{ k}\Omega/2} = 23.76$$

The vertical amplifier overall gain is thus:

$$A_v = A_{v1} \cdot A_{v2} \cdot A_{v3} = (10.3) \cdot (10.5) \cdot (23.76) = 2570$$

The deflection-plate sensitivity must therefore be $2570 \cdot (10 \text{ mV/div}) = 25.7 \text{ V/div}$. For 8 vertical divisions, the voltage range must be at least 206 V. The output of each side can change by $\pm 100 \text{ V}$. Thus the total deflection range is $\pm 200 \text{ V}$ or 400 V, corresponding to 2 screens of range.

Next time, I will give my list of deficiencies and improvements, giving you a month to inspect the circuit for design faults.

