

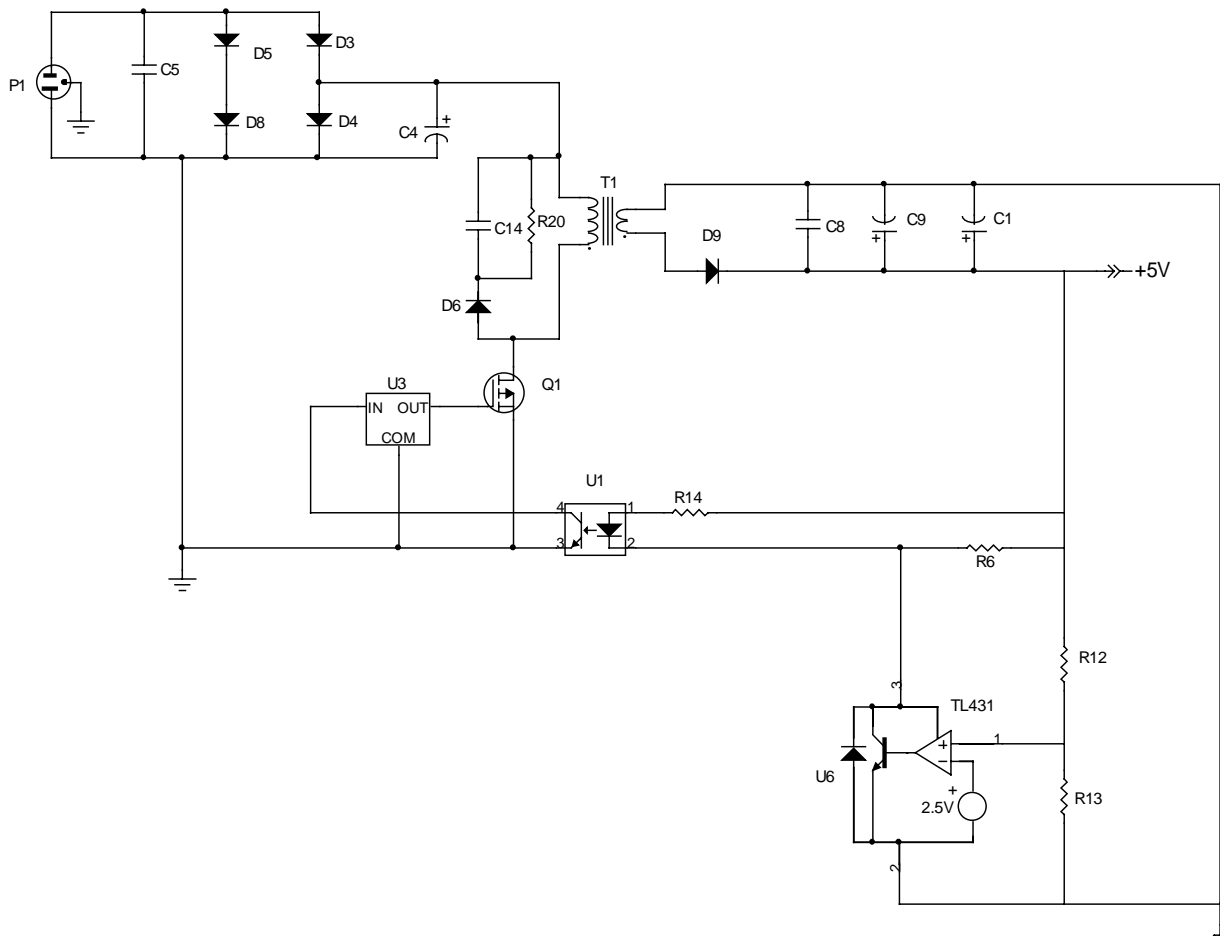
Flyback Transformer Leakage Inductance, Part 1

by Dennis L Feucht

Flyback converters are a common design choice for low-power (<100 W) converters. At low power it is more difficult to achieve high efficiency because otherwise negligible power losses, such as in the control circuitry, have a significant effect on efficiency. One of the main causes of power loss in flyback converters is due to the leakage inductance of the coupled inductor (transformer.) Minimization of leakage-inductance power loss is consequently of major interest in the design of flyback converters.

Generic Off-line Converter

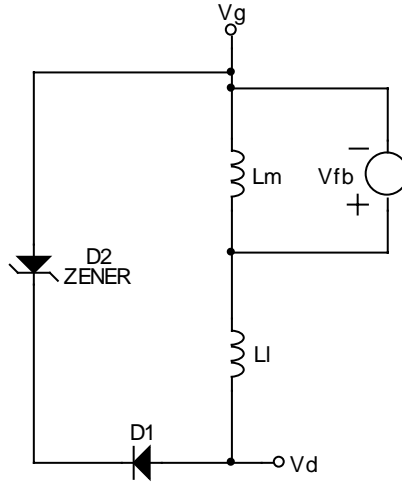
A generic low-power, off-line flyback converter is shown below. (The details of how flyback converters work will not be covered here.) Transformer T1 is the flyback magnetic component. The power switch is MOSFET Q1 and generic control IC is U3. Output voltage is compared by another IC, the TL431, and fed back to the primary side through optoisolator U1.



Attention is directed toward the flyback leakage inductance clamp circuit, consisting of D6, C14 and R20. These components comprise an RC clamp. R and C can be replaced in low input voltage converters by a Zener diode, which maintains a constant clamp voltage while the primary winding defluxes.

Magnetics Circuit Model

The model for the simpler Zener clamp circuit is shown below. The primary winding inductance is decomposed into magnetizing inductance, L_m , and leakage inductance, L_l .



L_m couples to the secondary circuit where the large output capacitor holds the output voltage relatively constant; the output appears as a voltage source. Added to the secondary diode drop, this secondary winding voltage refers to the primary winding, by the turns-ratio, as the *flyback voltage*, V_{fb} . The flyback voltage couples across the mutual inductance, L_m , but not the primary leakage inductance.

When switch Q1 turns off, the current in both inductances will continue to flow somewhere. Mutual inductance current will divert to the secondary and flow through the V_{fb} source, with current decreasing at the rate of $-V_{fb}/L_m$. With Q1 off, the current through the leakage inductance has nowhere to go other than into the clamp, D1, D2. The voltage that occurs across the leakage inductance is the clamp voltage, $V_Z + V_D$, minus V_{fb} . For instance, if the turns ratio (N_p/N_s) is 8 and $V_s = V_D + V_o = 0.8 \text{ V} + 5.0 \text{ V} = 5.8 \text{ V}$, then $V_{fb} = 8 \cdot (5.8 \text{ V}) = 46.4 \text{ V}$. To deflux the leakage inductance quickly (for efficient current transfer to the secondary), the opposing voltage of the clamp across L_l must be significant. To choose a clamp voltage for clamp design, the transfer time of the primary current to the secondary winding is a major consideration.

Current Transfer Delay

Suppose the primary inductance is 3 mH and the coupling coefficient of the transformer is $k = 0.98$. Then the leakage inductance is:

$$L_l = (1 - k) \cdot L_p = (0.02) \cdot (3 \text{ mH}) = 60 \mu\text{H}$$

If the converter switching frequency is 100 kHz, then the switching period is $T_s = 10 \mu\text{s}$. The primary-to-secondary current transfer delay time, t_d , is:

$$t_d = L_l \cdot \frac{\hat{i}_p}{V_{CL} - V_{fb}}$$

where the peak primary current (when Q1 turns off) is divided by the clamp voltage minus the flyback voltage. The design goal is to maximize transfer efficiency by minimizing t_d to be a small fraction of T_s . Usually the peak primary current is given for a per-cycle peak-current (current-mode) controller. And the turns ratio is set by optimizing the duty ratio over the input

voltage and load current ranges. This sets the flyback voltage. Transformer design results in L_l . Choice of clamp voltage remains: The higher V_{CL} the shorter t_d . Component voltage ratings -- especially that of the power switch -- limit the choice of how high V_{CL} can be made.

Commercially available Zener diodes in the 1 W to 5 W range are also limited in their upper voltages to about 200 V, but usually must be kept below 50 V by power limitations.

Assume the peak primary current is 0.25 A. Then the transfer delay time can be calculated given various values of clamp voltage. For $V_{CL} = 60$ V, t_d is 1.04 μ s, or over 10 % of the switching period. For a higher clamp voltage of 100 V:

$$60 \mu\text{H} \cdot \frac{0.25 \text{ A}}{100 \text{ V} - 46.4 \text{ V}} = 280 \text{ ns}$$

or 2.8% of the switching period. But 100 V Zeners begin to be expensive and have limited current ratings. A 1-W, 100-V Zener is limited to an rms current of 10 mA. The current at 0.25 A for 2.8 % of the time is about 42 mA. Consequently, Zener power requirements can become large -- larger than feasible -- quickly.

Closure

The larger V_Z is made, the shorter the transfer delay. The limit is the sizing of Zener diodes. The larger the Zener voltage, the smaller the peak allowable current for the same peak power rating. For low-power converters, it makes little sense to include an expensive high-power, high-voltage Zener. Practical low-power converter limits are reached around 50 V. For off-line converters, with their high primary voltages (375 V dc at the high end of the universal line range), the turns ratio is large, making the flyback voltage large. Because the clamp voltage must significantly exceed V_{fb} , it too must be large. Zeners become impractical for universal-input, off-line converters. This leads to the RC clamp. But before it is analyzed, current transfer to the secondary will be examined in more detail in Part 2 so that the detrimental effects of t_d can be fully appreciated.

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