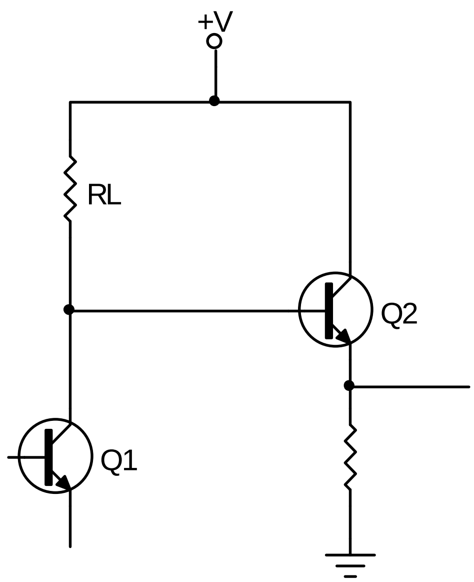
Bootstrap Speed-Up Circuit

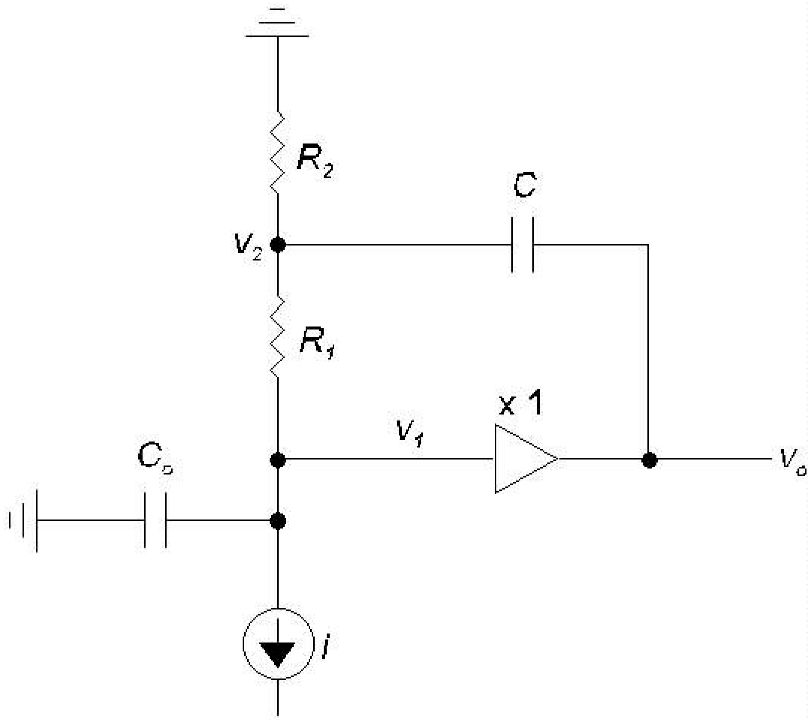
by Dennis L Feucht

How do you increase the speed of an amplifier without increasing its power consumption? Amplifier bandwidth can be extended by a simple technique that requires no inductors or complicated adjustments. It is applicable to both IC or discrete transistor amplifiers and has been used in wideband oscilloscope amplifiers. Though simple in principle, engineering derivations are not readily available in the literature and this TechNote presents the circuit, its description, analysis, and design comments.

In its simpler form a collector- or drain-loaded transistor amplifier, as shown below, has a single load resistor, R_L, followed by a buffer amplifier, usually an emitter- or source-follower. The buffer stage keeps the output from directly loading R_L by providing current gain and approximately a ×1 voltage gain. This two-stage cascaded amplifier is typical in high-speed circuit design as a place to start before increasing amplifier "speed" (bandwidth).



What can mainly limit speed is the capacitance, *Co*, at the collector node of the first stage. It forms a time constant with R_L that slows the dynamic response. To increase speed it is possible to introduce various inductive peaking techniques. (See the volume on High-Performance Amplifiers in my Analog Circuit Design e-book, available at http://www.innovatia.com, for those details.) However, for IC and some discrete design, inductors are problematic.



A speed-up technique that uses capacitance instead is the bootstrap speed-up circuit shown above, where Q1 has been replaced by a current source, *i*, and the Q2 stage by an ideal ×1 buffer amplifier. R_L has been split into R_1 and R_2, and a bootstrap capacitor, *C*, added between the output and the split-R_L node.

The idea behind this circuit is that if the voltage at the top of R_1 can track the voltage at the bottom of R_1, the voltage across R_1 will be zero. Then none of *i* will be diverted into the load resistance. With all of *i* flowing into *Co*, it charges faster and the circuit response is quicker. In effect, *C* bootstraps the voltage across R_1 to accomplish this, and the buffer amplifier output has the needed current drive to provide R_2 current.

To analyze the dynamic response of this circuit, the s-domain (pole-zero) expressions need to be derived. The full analysis takes some algebraic doing. To provide further insight into the circuit, and guidance for checking the full result later, a simpler analysis omits *Co*. By setting *Co* = 0, the output-node voltage is:

$$v_1 = i \cdot \left(R_1 + R_2 \,||\, \frac{1}{sC} \right) + v_o \cdot \left(\frac{R_2}{R_2 + 1/sC} \right);\ v_o = v_1$$

After some algebraic simplification, this becomes:

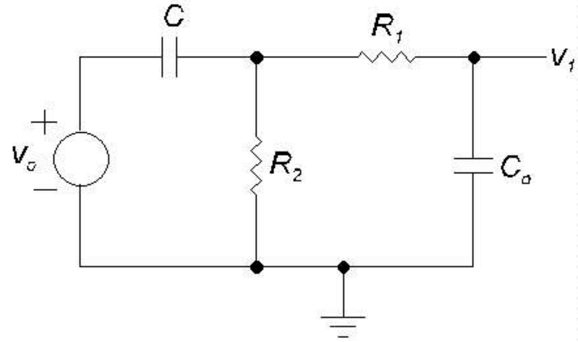
$$v_1 = i \cdot \left(R_1 + \frac{R_2}{sR_2C + 1} \right) + v_o \cdot \left(\frac{sR_2C}{sR_2C + 1} \right)$$

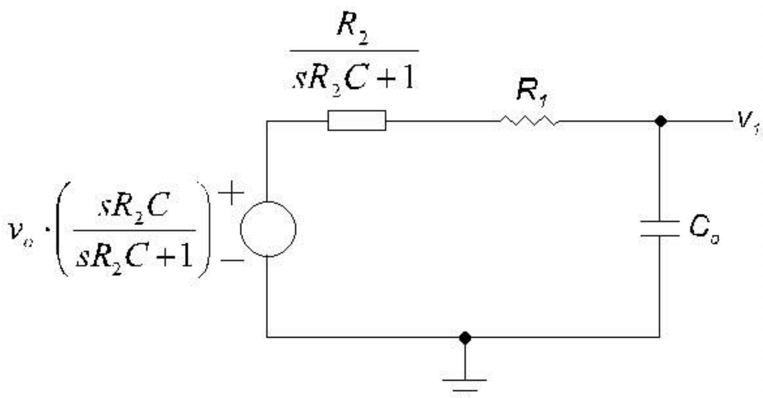
Then the first-stage amplifier gain, a transresistance (current in, voltage out), is:

$$\frac{v_o}{i} = \frac{R_1 + \dfrac{R_2}{sR_2C + 1}}{1 - \dfrac{sR_2C}{sR_2C + 1}} = (R_1 + R_2) \cdot (s[R_1 \,||\, R_2] \cdot C + 1)$$

From this result, $R_L = R_1 + R_2$ is the static gain, followed by a zero at $z = -1/(R_1 \,||\, R_2) \cdot C$. The absence of a pole is due to bootstrapping. The pole formed by R_2 and *C* is cancelled by the ×1 buffer gain. If its gain were a value of *K* other than one, a finite pole would appear at $s\,(K - 1) \cdot R_2 \cdot C + 1$.

Now include *Co* in the analysis such that $Co \neq 0$. Then the circuit can be modeled as shown below.





The input current source is omitted, but attaches to the output node, at v_1. The two-loop circuit reduces to a single loop by Thevenizing v_o, C, and R_2, as shown in the second circuit. Then superposition of the two sources, v_o and i, results in the following two equations:

$$v_1 = v_o \cdot \left(\frac{sR_2C}{sR_2C+1}\right) \cdot \left(\frac{sR_2C+1}{s^2(R_1R_2CC_o) + s[(R_1+R_2)\cdot C_o + R_2C]+1}\right), i = 0$$

$$v_1 = i \cdot \left(\frac{1}{sC_o} \parallel (R_1 + R_2 \parallel 1/sC)\right) = i \cdot (R_1+R_2) \cdot \frac{s(R_1 \parallel R_2)C+1}{s^2R_1R_2CC_o + s[(R_1+R_2)C_o + R_2C]+1}, v_o = 0$$

The first equation simplifies quickly to:

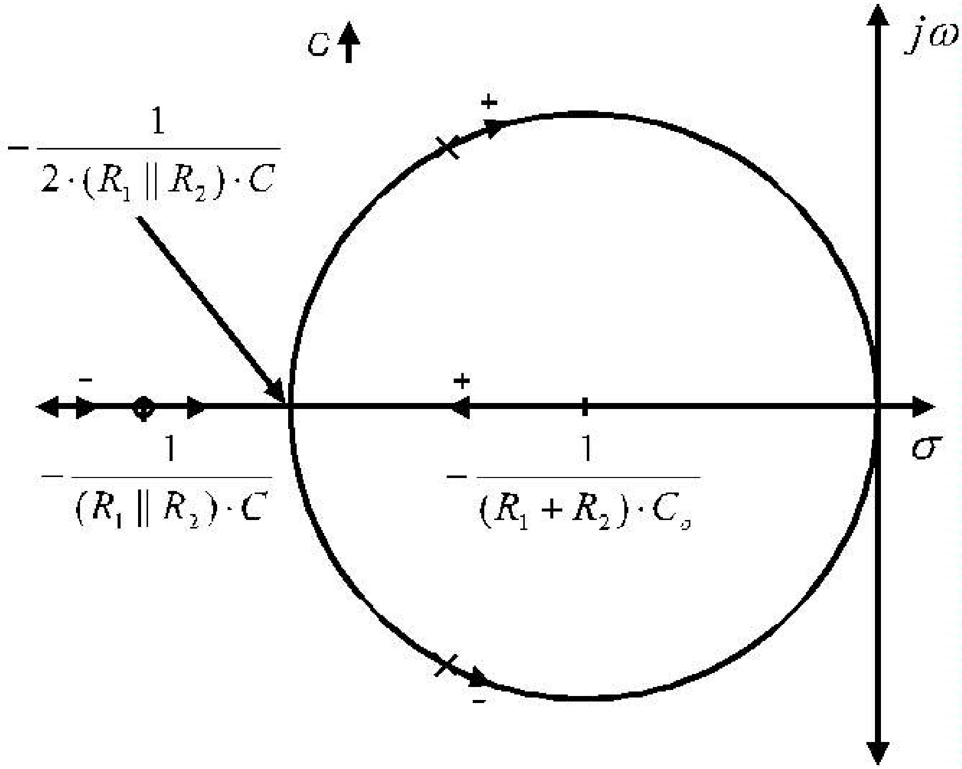
$$v_1 = v_o \cdot \left(\frac{sR_2C}{s^2(R_1R_2CC_o) + s[(R_1+R_2)\cdot C_o + R_2C]+1}\right), i = 0$$

Applying the buffer condition, $v_o = v_1$, and by superposition:

$$\frac{v_o}{i} = (R_1+R_2) \cdot \frac{s(R_1 \parallel R_2)C+1}{s^2R_1R_2CC_o + s(R_1+R_2)C_o + 1}$$

The bootstrap capacitor, *C*, provides for the additional zero. Without it ($C = 0$), the uncompensated circuit pole remains at $-1/(R_1 + R_2)\cdot Co$, as in the uncompensated amplifier. The design question is now one of determining the optimal value of *C* and the split between R_1 and R_2.

The contour (not root locus) plot of the poles of this circuit is shown below. *C* appears only in the quadratic term, leading to a locus which varies with increasing *C* as shown.



The conjugate poles are marked with their polarities to show that the positive pole originates at the center of the pole-pair circle, $-1/(R_1 + R_2)\cdot C_o$ (the pole location of the uncompensated amplifier), and the negative pole at -∞. The contour plot itself begins at the frequency of the zero, $-1/(R_1 \parallel R_2)\cdot C$, and at the circle center. As *C* increases, the poles move toward each other and meet at $-½(R_1 \parallel R_2)\cdot C$ before splitting off the real axis and eventually terminating at the origin for excessively large (infinite, shorted) *C*. For equal poles on the real axis:

$$2(R_1 \parallel R_2)\cdot C = \tfrac{1}{2}\cdot(R_1 + R_2)\cdot C_o$$

from which the design constraints are obtained: $R_1 = R_2$ and $C = C_o$.

Closure

Optimal amplifier response usually has the poles off the real axis for a compromise between time- and frequency-domain response performance. For maximally-flat envelope delay (MFED), the pole angle is 30°. The relevant formulae are as follows. The damping factor is:

$$\zeta = \frac{b}{2\cdot\sqrt{a}} = \frac{1}{2}\cdot\sqrt{\frac{(R_1 + R_2)\cdot C_o}{(R_1 \parallel R_2)\cdot C}}$$

where the pole angle is:

$$\phi = \cos^{-1}\zeta$$

The pole radius is:

$$\omega_n = \frac{1}{\sqrt{a}} = \frac{1}{\sqrt{R_1 R_2 C C_o}}$$

Then for a pole angle of $\phi = 30°$, $\zeta = \cos 30° = \sqrt{3}/2$ and:

$$\frac{(R_1 + R_2)\cdot C_o}{(R_1 \parallel R_2)\cdot C} = 3$$

Then given R_1, R_2, and an estimate for *Co*:

$$C = \frac{(R_1 + R_2)\cdot C_o}{3\cdot(R_1 \parallel R_2)}$$

For $R_1 = R_2$, then:

$$C = \frac{4}{3}\cdot C_o$$

Because *Co* is an undesirable parasitic circuit element, it is typically both small and takes on a range of possible values. Because of its only approximate value, *C* might need to be adjustable to tune the pole angle for optimal response.

C is also small, approximately the value of *Co*. Consequently, small-variable-capacitance methods might need to be applied. One simple discrete-circuit approach is to use what used to be called a "gimmick". Twist a length of insulated wire, strip and solder one pair of ends as *C* terminals, and snip the length of the pair for optimal *C*. Then varnish or glue *C* to retain its geometry and its *C* value. This works for relatively slow high-speed circuits. Better methods can also be applied. If approximate dynamic behavior is adequate, or by using a response trim elsewhere, no adjustment is needed. In this case, a circuit-board or IC capacitance, though approximate, can be sufficient.