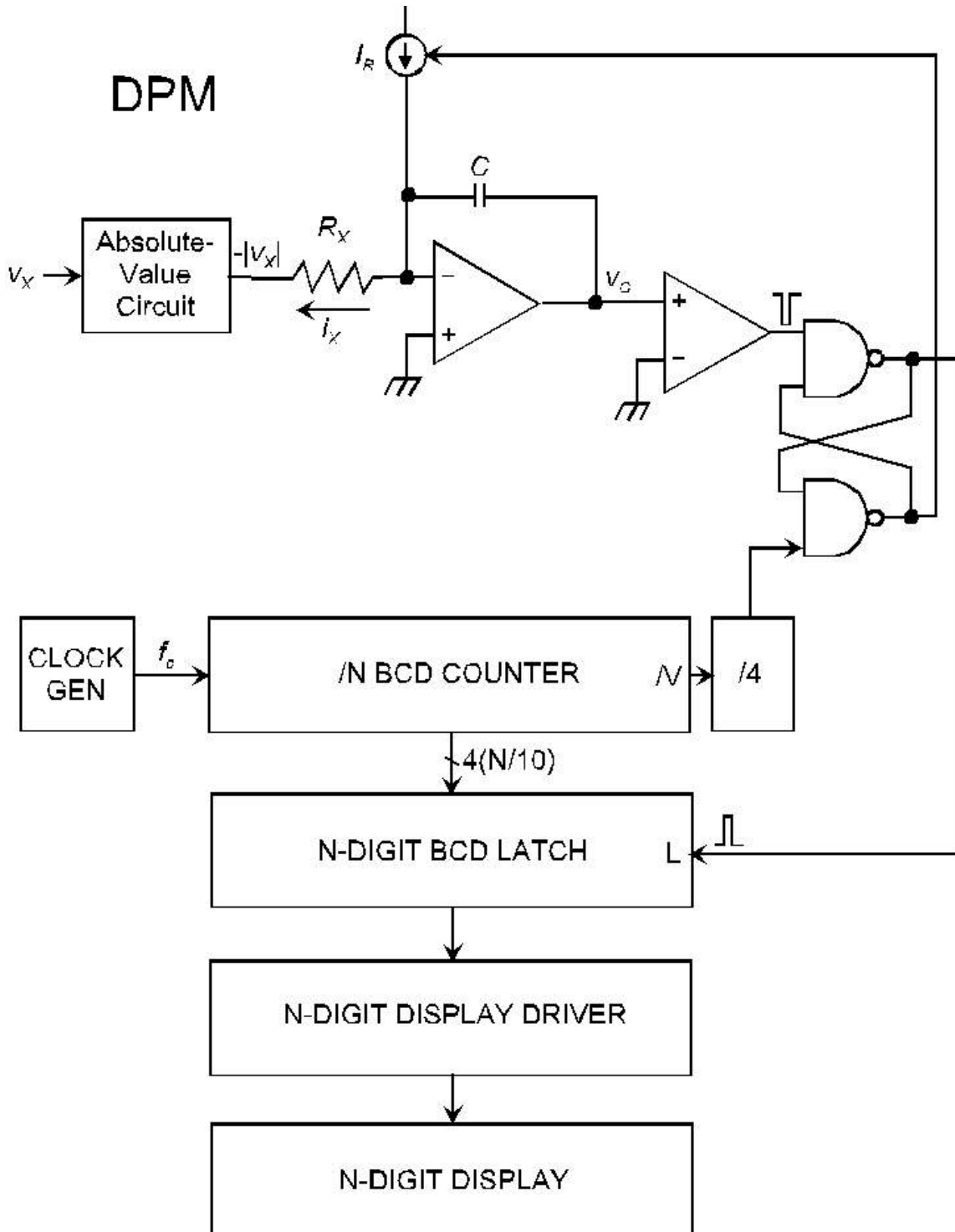


Design And Build A Simple DPM

by Dennis L Feucht

Digital panel meters (DPMs) are usually used as dedicated digital voltmeters (DVMs) and are also the core of digital multimeters (DMMs). This project entails design derivations and implementation of a simple DPM. Although DPMs are low-cost and available as a single IC, this project presents a case study of a design for new analog engineers of a mixed-signal device. The core of the project is a modified dual-slope analog-to-digital converter (ADC). The basic converter scheme is shown below.



DPM Design

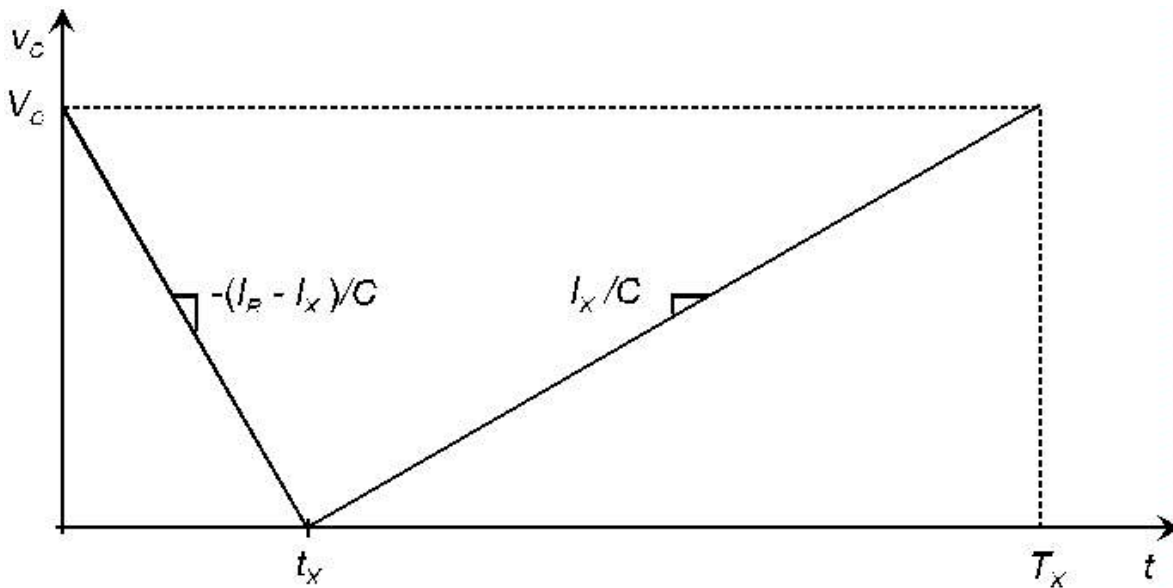
In the above functional diagram the unknown voltage to be measured, v_X , will be allowed a bipolar range of $\pm V_X$, where V_X is the full-scale magnitude of v_X . The absolute-value circuit (a precision rectifier) output for both positive and negative voltages are negative voltages in the range of 0 V to $-V_X$. Its output is therefore $-|v_X|$. This voltage is converted to a current by the input resistor of the following op-amp integrator, for which:

$$i_X = \frac{|v_X|}{R_X}$$

and for the \pm full-scale value:

$$I_X = \frac{V_X}{R_X}$$

The integrator is inverting, and the negative i_X causes the output, v_C , to increase. If i_X is constant, v_C ramps upward, as shown below.



The Digital Part

The chain of causation begins with the clock generator, a digital oscillator of frequency f_c . It drives the BCD counter chain. We will design a 3-digit DPM, requiring three decades of display count, or 1000. The overflow output of the counter, $/V$, is divided by 4, which resets the NAND-gate RS flop, causing the lower gate output to be set high. The reference current source, I_R , is switched on by the RS flip-flop (FF) output, and v_C integrates downward, as shown above. When it reaches 0 V, the comparator following the integrator outputs a low level, thereby setting the RS flop. The I_R source is turned off, the display latch is strobed to store the count at t_X , and only i_X is integrated. Then v_C ramps upward until the counter again overflows, at T_X , the measurement interval. This time is:

$$T_X = \frac{N}{f_c}$$

where, N is the number of counts of the total counter chain. For the three-digit display, $N = 4000$.

The full-scale t_x is only $\frac{1}{4}$ of T_x . This allows 100% over-ranging up to $T_x/2$. To use this additional range, a *half digit*, which is a ± 1 digit display letting the full-scale MSD of the reading be 1999, with a count range of 2000. In this case, the full-scale input, or V_x , must begin with a 2, such as 2 V. In our case we will not use this additional capability but, instead, design the input for $V_x = 10$ V.

Then the input range of the DPM is ± 10 V.

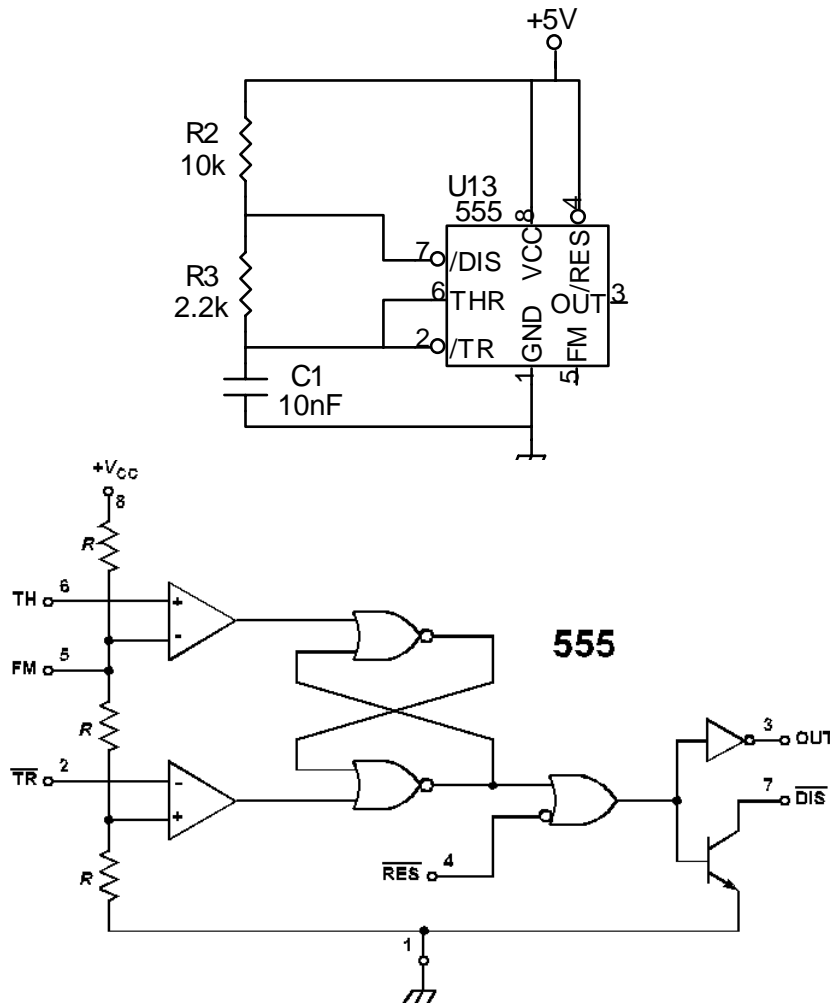
Another reason for full-scale t_x to be $\frac{1}{4} T_x$ is measurement stability. The v_C waveform is only stable – that is, it only converges to a stable waveform – when $t_x < T_x/2$. (This is derived in *Analog Circuit Design*, [Signal Processing Circuits volume] at <http://www.innovatia.com>.) The $\div 4$ counter following the BCD counter provides the additional measurement time, and places t_x at a count of 1000 out of 4000 total during the measurement cycle.

Another design decision is to have a measurement rate (or $1/T_x$) of 2.5 readings per second. Then $T_x = 400$ ms

$$\text{Then } f_c = \frac{N}{T_x} = \frac{4000}{400 \text{ ms}} = 10 \text{ kHz}$$

A design goal will be to implement the DPM using legacy ICs: well-established, enduring components available from multiple suppliers. Also, to keep the design simple (though somewhat compromised in performance), low-cost commodity parts will also be used and frequently-appearing component values chosen.

The oscillator is implemented with a 555 timer, as shown in the circuit diagram of the completed design, below.



The /TR (trigger not) and TH (threshold) comparators are internally connected to switch at 1/3 and 2/3 of V_{CC} , respectively. R2 provides current from V_{CC} to charge C1 until the TH comparator changes output state, causing the timer output to be low and the open-collector /DIS (discharge not) output (which is of the same phase as the OUTput) to pull low. This isolates R2 from the timing circuit and sinks timing current from R3, discharging C1 until 1/3 V_{CC} is reached. The TR comparator then asserts, setting the output (OUT) high and turning off the /DIS BJT to start another cycle.

The C1 voltage waveform is an exponential sawtooth that oscillates between 1/3 and 2/3 V_{CC} . The time it takes to traverse between these two voltages is derived from the equation for an exponential waveform:

$$v_C = V_T \cdot (1 - e^{-t/RC})$$

where, V_T is the asymptotic *target* voltage that v_C approaches in time. For v_C starting at 1/3 V_{CC} and ending at 2/3 V_{CC} , the target voltage is V_{CC} and the risetime of v_C is:

$$t_H = -RC \cdot \ln\left(1 - \frac{v_C}{V_T}\right) = -RC \cdot \ln\left(1 - \frac{\frac{2}{3} \cdot V_{CC}}{V_{CC}}\right) - \left[-RC \cdot \ln\left(1 - \frac{\frac{1}{3} \cdot V_{CC}}{V_{CC}}\right)\right] = -RC \cdot \ln\left(\frac{1}{2}\right) = RC \cdot \ln 2 \cong (0.693) \cdot RC$$

For the t_H half-cycle, $R = R2 + R3$ while for the t_L half-cycle, $R = R3$. Then the total period is:

$$T_c = \frac{1}{f_c} = t_H + t_L = (R2 + 2 \cdot R3) \cdot C1 \cdot \ln 2 \cong (0.693) \cdot (R2 + 2 \cdot R3) \cdot C1$$

Applying the given T_X :

$$T_c = \frac{T_X}{N} = \frac{400 \text{ ms}}{4000} = 100 \mu\text{s}$$

the clock frequency is:

$$f_c = 10 \text{ kHz}$$

Substituting for T_c :

$$(R2 + 2 \cdot R3) \cdot C1 = \frac{100 \mu\text{s}}{\ln 2} \cong 144.3 \mu\text{s}$$

In keeping with the design style of choosing commonly-available components, let $C1 = 10 \text{ nF}$, a common decade value. Then:

$$R2 + 2 \cdot R3 = \frac{144.3 \mu\text{s}}{10 \text{ nF}} = 14.43 \text{ k}\Omega$$

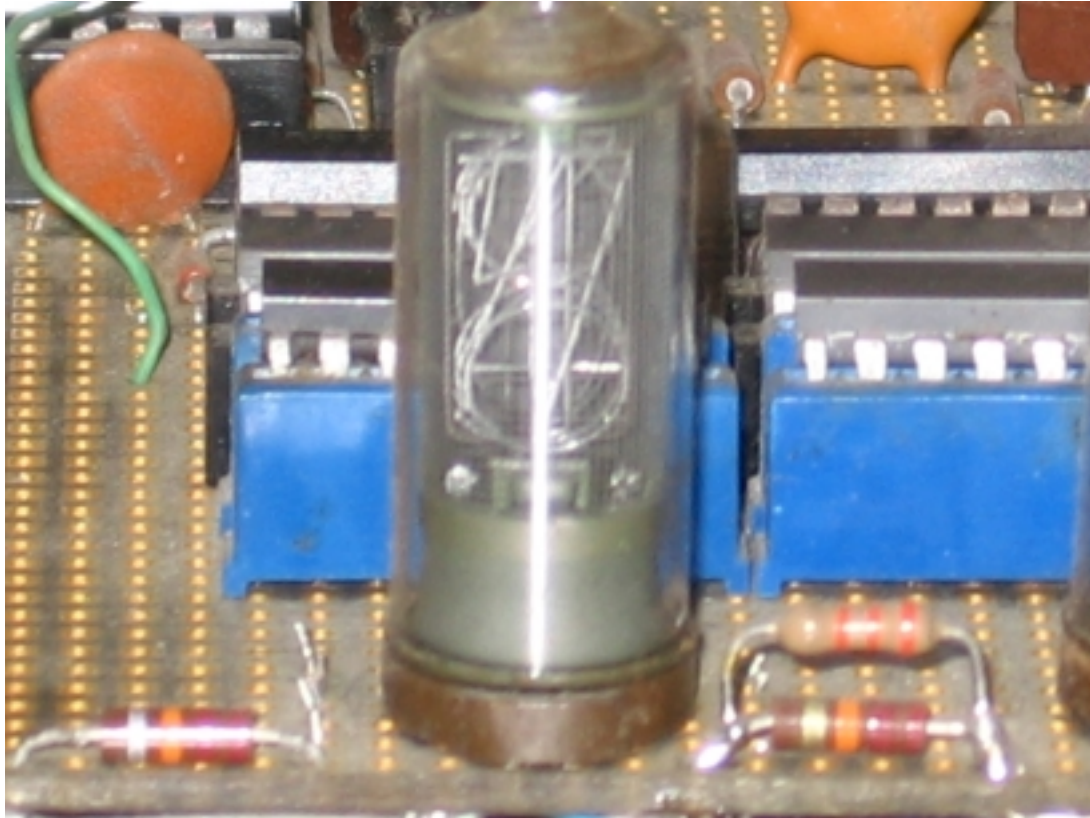
Choose a decade value for R2 of 10 k Ω , and:

$$R3 = \frac{14.43 \text{ k}\Omega - 10 \text{ k}\Omega}{2} = 2.21 \text{ k}\Omega \rightarrow 2.2 \text{ k}\Omega$$

The chosen component value is the closest 5 % value and is also close to the calculated value. As we will see, f_c does not affect the accuracy of the measurement (only affects T_X), and thus need not be accurate.

The digital part of the DPM can be implemented with a single multi-decade counter-latch-display-decoder-driver IC such as the Intersil ICM7225 or a 40110 CMOS IC for each digit of 7-segment LED displays. The digital parts used in this implementation were chosen in 1971 from the 74LS00 or 74HC00 series. The 3 BCD counters are 74LS90, the 3 latches are 74LS75, and the 3 display drivers are 74141 because the choice of display (for something a little different nowadays) is cold-cathode gas-discharge displays, or Nixie tubes, as Burroughs called them.

These are essentially neon bulbs containing metal shapes for each of the 10 numerals. One of ten is selected as the cathode by pulling it to ground, and the anode mesh in back of the tube completes the circuit to 170 V. Unselected cathode drivers must withstand up to 60 V. The selected numeral glows orange. A close-up photo of an unlit Nixie tube is shown below.



The Nixie-tube choice violates the design heuristic to stay with common parts. These displays are available, though antiquated and harder to get than 7-segment LED displays, which would be the preferred choice.

For LED displays, we must decide on a 7-segment LED driver. The standard TTL 74142 combines counter, latch, decoder and display driver into one IC for Nixie tubes, combining 3 MSI ICs into one per digit of display.

This TTL IC, however, was not carried forward into newer families of TTL (nor was the 74141), presumably because of the anticipated demise of Nixie tubes as displays. Consequently, the circuit diagram of the DPM design retains the Nixie tubes, though the more optimal choice nowadays is a single ICM7225, which needs few additional parts to provide the core digital part of the design.

The ÷4 counter following the display part of the total counter chain is still needed, however. It is implemented here with JK flops, though for the ICM7225, which uses the rising edge of the clock, a 74HCT74 D flop, which is also clocked on the rising edge, would be substituted. So much for the digitally-intensive part of the design.

To be continued...

