

# Build Your Own Waveform Recorder

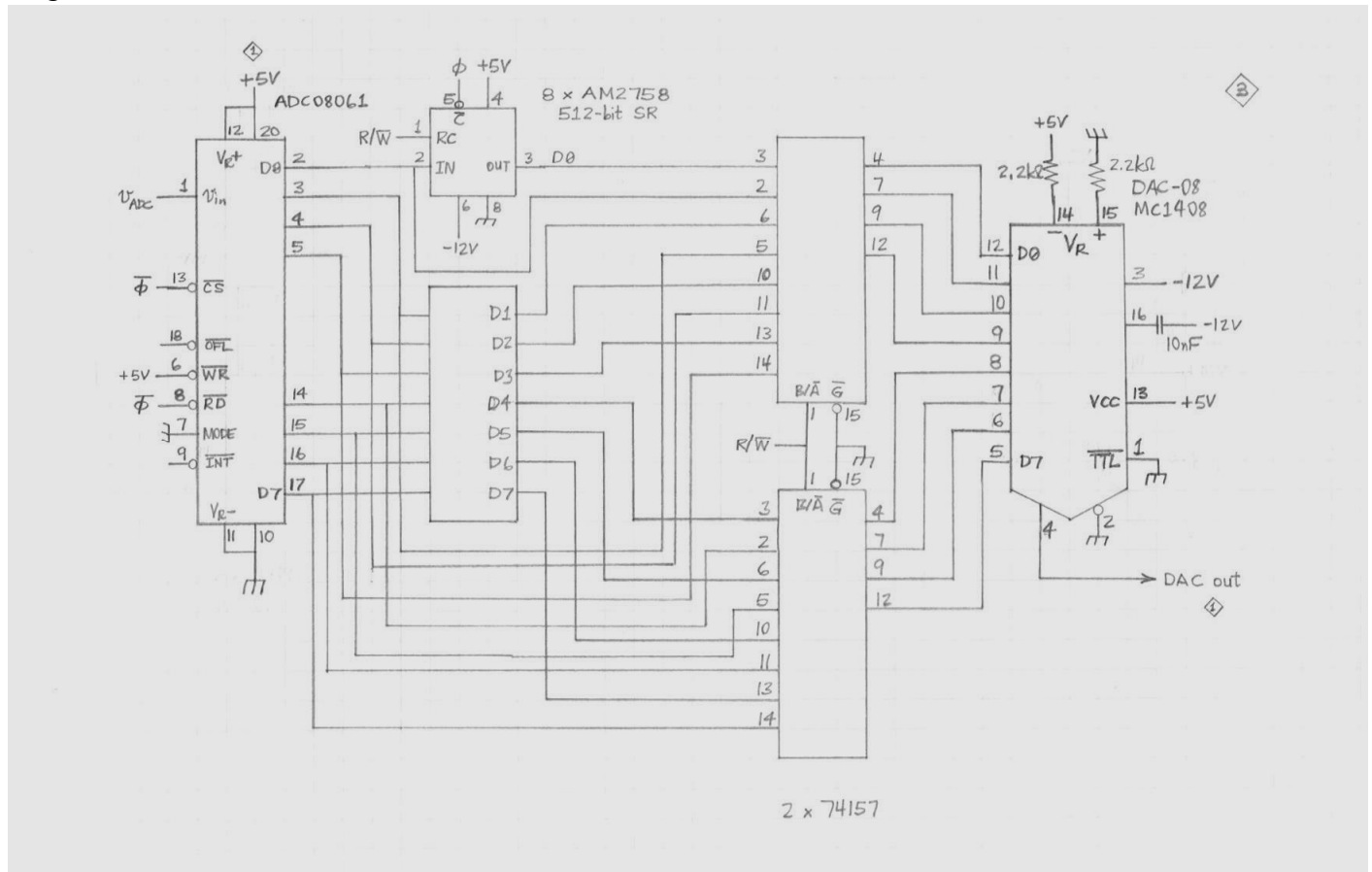
## Part 2

by Dennis L Feucht

Continuing the waveform recorder project, we move on to the core circuitry.


### ADC, Waveform Memory And DAC

Mixed-signal components dominate the digitizer, memory and playback DAC, as shown in the circuit diagram below.



The ADC is a low-performance NSC ADC08061, an 8-bit ADC. Its 8 digital output lines each drive a 512-bit serial shift-register memory. Serial memory can be replaced by RAM and the sample counter lines used for addressing. However, this something a little different, though finding the AM2758 p-MOS parts might be a challenge. Serial memory vastly reduces the board traces (or wires) by implicitly addressing samples through the order they occur in the shift-register stages. Serial shift-register memory should be inherently faster than RAM (though not in this case!) because it does not have address-decoding delay. It is a more optimum form of memory for this application.

A copy of the front page of the ADC08061 specifications is shown below, taken from a 1991 National Semiconductor data book. The specifications show that it is capable of digitizing at a 1 MHz rate. Nowadays, a comparable IC might have a sampling rate 50 times that of this part. Yet most comparable ADCs with parallel-bit output will function satisfactorily.


February 1991

## ADC08061/ADC08062/ADC08064/ADC08068 500 ns A/D Converter with S/H Function and Input Multiplexer

### General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08061, ADC08062, ADC08064, and ADC08068 CMOS A/D converters offer 500 ns conversion time, internal sample-and-hold (S/H), and dissipate only 100 mW of power. The ADC08062, ADC08064, and ADC08068 include, respectively, a 2-, 4-, and 8-channel multiplexer. The ADC08061/2/4/8 family performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LSBs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08061/2/4/8 family can perform accurate conversions of full-scale input signals at frequencies from dc to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, these parts have been designed to appear as a memory location or I/O port without the need for external interfacing logic.

### Key Specifications

■ Resolution	8 bits
■ Conversion Time	500 ns max (WR-RD Mode)
■ Full Power Bandwidth	300 kHz
■ Throughput rate	1.5 MHz
■ Power Dissipation	100 mW max
■ Total Unadjusted Error	$\pm 1/2$ LSB and $\pm 1$ LSB

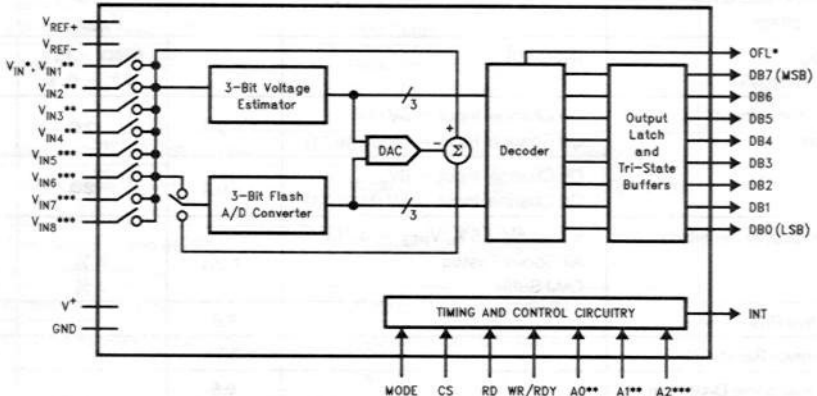
### Features

- 1, 2, 4, or 8 input channels
- No external clock required
- Analog input voltage range from GND to V+
- Overflow output available for cascading (ADC08061)
- ADC08061 pin-compatible with the industry standard ADC0820
- ADC08064 and ADC08068 are pin compatible with AD7824 and AD7828, respectively

### Applications

- Mobile telecommunications
- Hard disk drives
- Instrumentation
- High-speed data acquisition systems

### Block Diagram



\*ADC08061  
 \*\*ADC08062, ADC08064, and ADC08068  
 \*\*\*ADC08064 and ADC08068  
 \*\*\*\*ADC08068

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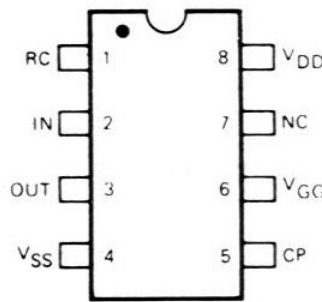
TRI-STATE® is a registered trademark of National Semiconductor Corporation.

The 8 ADC digital bit outputs each drive a 512-bit serial shift-register memory. If you replace the serial memory with RAM, the sample counter lines can be used for RAM addressing.

The AMD AM2758 serial shift-register memory is described in the following page lifted from its spec-sheet.

AMD AM2758

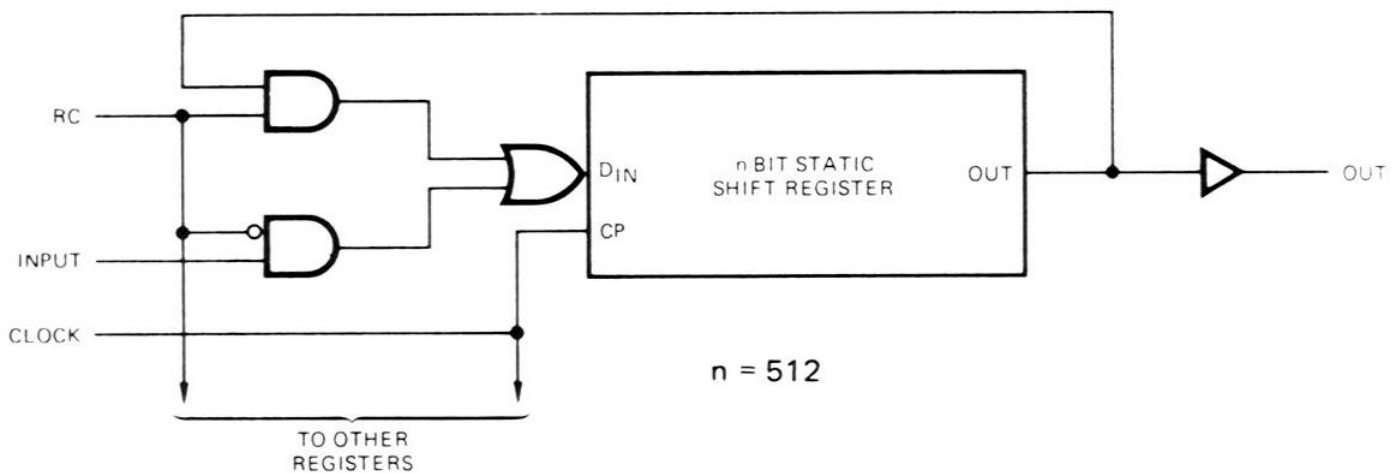
PIN CONFIGURATION



LOGIC SYMBOL

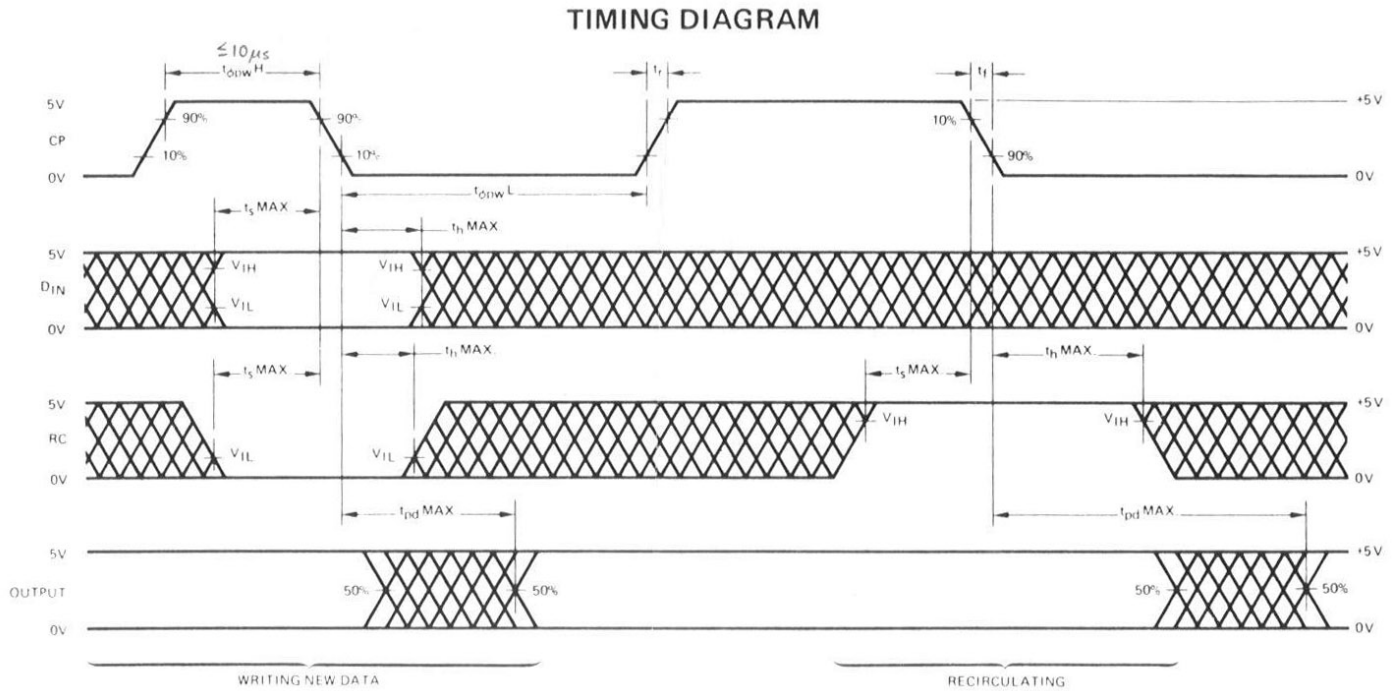


LOGIC DIAGRAM



The logic diagram shows its optimality for this application, for the input selection logic can be use to either recirculate the waveform for playback or select the ADC input while recording. As a p-MOS part, it needs a -12 V VGG supply for gate biasing. The 512-bit length, while somewhat short for a commercial product,

gives an acceptable horizontal waveform resolution. The timing for the memory, from the AMD data book, is shown below. The cross-hatched segments are “don’t care”.



There is nothing very subtle about the timing. Setup times for  $D_{IN}$  must be sufficient before the trailing (falling) edge of the clock (CP) transitions. For analog engineers needing some basic experience with digital, sequential logic and its timing might benefit by building this recorder using the shift-register parts.

After the memory, two 74157 multiplexers select between ADC output and memory for the DAC input, depending on whether memory read (playback) or write (acquisition) is occurring. During acquisition the waveform is output through the DAC for display so that for slow sampling rates, the user can see whether a desirable acquisition is occurring.

The DAC itself is a low-cost, bipolar, 8-bit DAC. It has no outstanding features that would fix it in your head; but of this unpossessing DAC, there’s something to be said. Its outputs (the complement is unused and grounded) are from open collectors below ground in voltage range, and can directly drive the inverting input of an op amp. Schematic sheet 1 of Part 1 shows this interface; the noninverting input is grounded. For this simple coupling, the op amp input bias current is compensated by making the noninverting input external resistance be equal in value to the feedback resistance. Then the two inputs have the same resistance. In this design, the error was considered negligible and the resistor was not added between the noninverting input and ground.

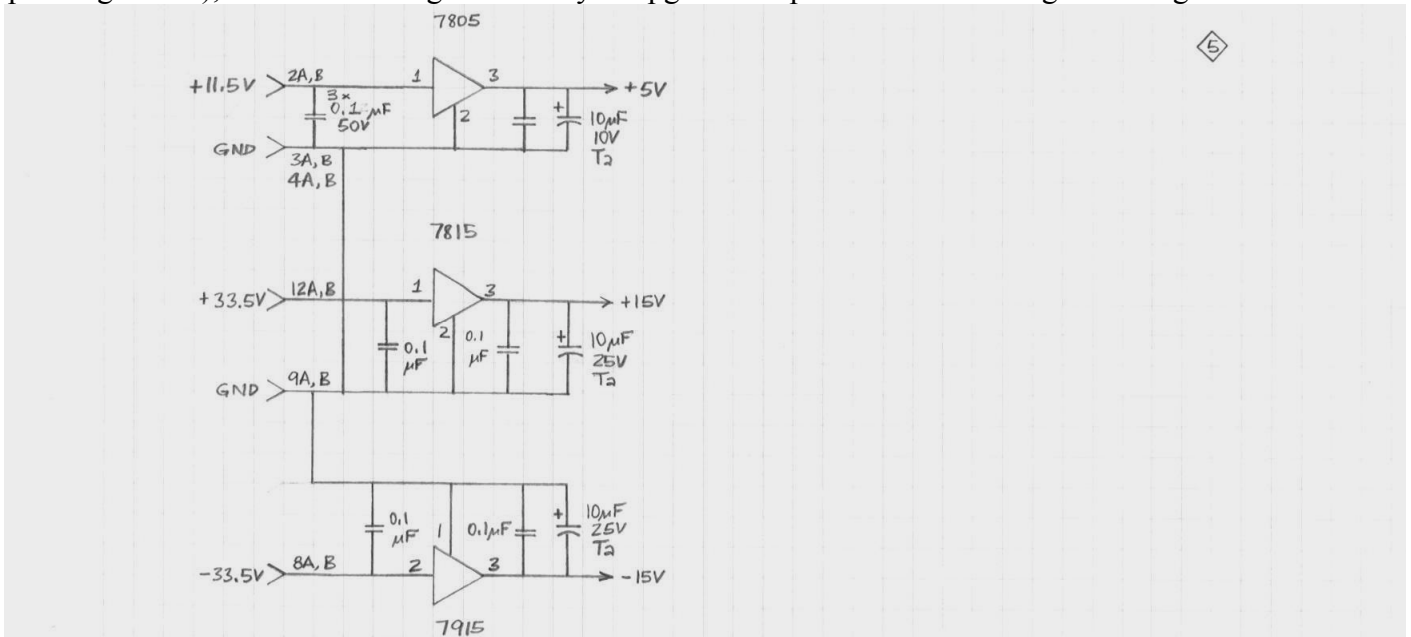
### Some Additional Digital Circuitry

To complete the WR502, some additional logic circuitry is required, as shown in sheet 4. First, the front-panel STORE pushbutton is debounced using an RS flop of NAND gates. Following it is a 7476 JK flop, clocked on the negative (falling) edge. The RS flop outputs a low level when the STORE button has been pushed to its momentary-contact state, grounding 7400 (B), pin 5. When released, it again grounds the pin 1 input, forcing the output high. The output of the 7476 flop depends on the R/W state. If reading (in playback mode), J is high. K is always low. Then Q is set high and  $\bar{Q}$  low.



current ratings on each need not exceed an ampere, and can be substantially less if you upgrade the logic for newer parts.

If you use 7800 and 7900 series linear regulators, be sure to provide adequate capacitor bypassing at both input and output, especially for the negative (7915) regulator. These parts are essentially power op-amps with a reference-voltage input and both load and input affect the dynamics of the feedback loops within them. If you want to push for a low-power (maybe even battery-operated) WR501, I recommend using the newer generation of linear regulators (LDO regulators) driven by an efficient switching supply. The linear post-regulators provide a cleaner and more stable output than the multi-output switcher (unless it already has post-regulation), which can be significant if you upgrade the performance of the given design.



## Closure

This modest-performance waveform recorder and playback unit has little in the way of functional subtlety and, consequently, offers both a quick project for technical people looking for bench experience and a starting point for exercising and improving new design skills. It illustrates the basic functions found in digital storage oscilloscopes (DSOs). The simplicity of the circuit design lets newly graduated engineers or technicians comprehend it to sufficient depth to master the concepts involved, then imagine various improvements. Please try them when you do, for the development of creativity is essential to the engineering skill-set. This design provides plenty of opportunity for improvement and the effort is not overbearing relative to the amount of work required to construct and functionalize the given design. And if you do so, please email me about what you did. Perhaps it will merit a Part 3 for this project.

