External Circuit Effects on High-Speed ADC Inputs

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The high-speed analog-to-digital converters (ADC) that convert an analog signal voltages into binary coded signals at sampling rates greater than 1 Msample/s have been in fast development and are being widely used in many advanced systems in communications, measurements and image processes. These systems are continuously creating a great demand on the speed and resolution of the ADCs to improve the system quality and hardware complexity. For example, an image processing system requires an ADC having 12-bit resolution or better at sampling rate above 60 Msample/s to achieve a good signal-to-noise ratio (SNR) and linearity. A measurement system requires an ADC having not only high SNR but also a good spurious free dynamic range (SFDR) at high dynamic sampling speeds to maintain high accuracy and flexibility of the measurement.

A wideband sampling system requires an ADC having a sampling rate as fast as possible to avoid sampled signal distortion without an expensive anti-alias filter in the front end. Similarly in a wireless base station it is preferable to have an ADC having enough speed that an intermediate frequency (IF) signal can be sampled directly to eliminate a down conversion stage. The ADC used for these applications is typically designed to have good resolution and high sampling speed with pipeline architecture, providing SNRs of better than 70 dB and SFDRs better than 85 dB.

For a high-speed ADC the sampling speed, SNR, SFDR and THD (Total harmonic distortion) are the basic parameters used to characterize the dynamic performance of the ADC. Because the high-speed ADC is such a precise device these parameters are the function of many factors -- externally as well and internally.

The internal factors mainly include design architecture and process. The external factors include signal source, signal input circuit, clock source, output digital load, power supply decoupling, reference bypassing and board layout. A signal input circuit is critical to the ADC performance. Poor input signal conditions such as large input signal source noise, source nonlinearity, source impedance mismatch, asymmetric input signal paths and large capacitive loads, etc can significantly degrade the dynamic performance of the high-speed ADC.

In order to achieve the best performance of a high-speed ADC, the input circuit must be carefully examined. In this article we focus on the external input circuitry for the high-speed ADC and introduce a few input circuits to examine how they affect the ADC performance. For a better understanding of those effects the basic theory of operation of a high-speed ADC is also introduced in this article.

Fundamental Theory of High Speed ADC

A high-speed ADC usually consists of six sections: the input stage, the output stage, the ADC core, digital error correction, reference voltage circuitry and clock circuitry (Fig. 1).

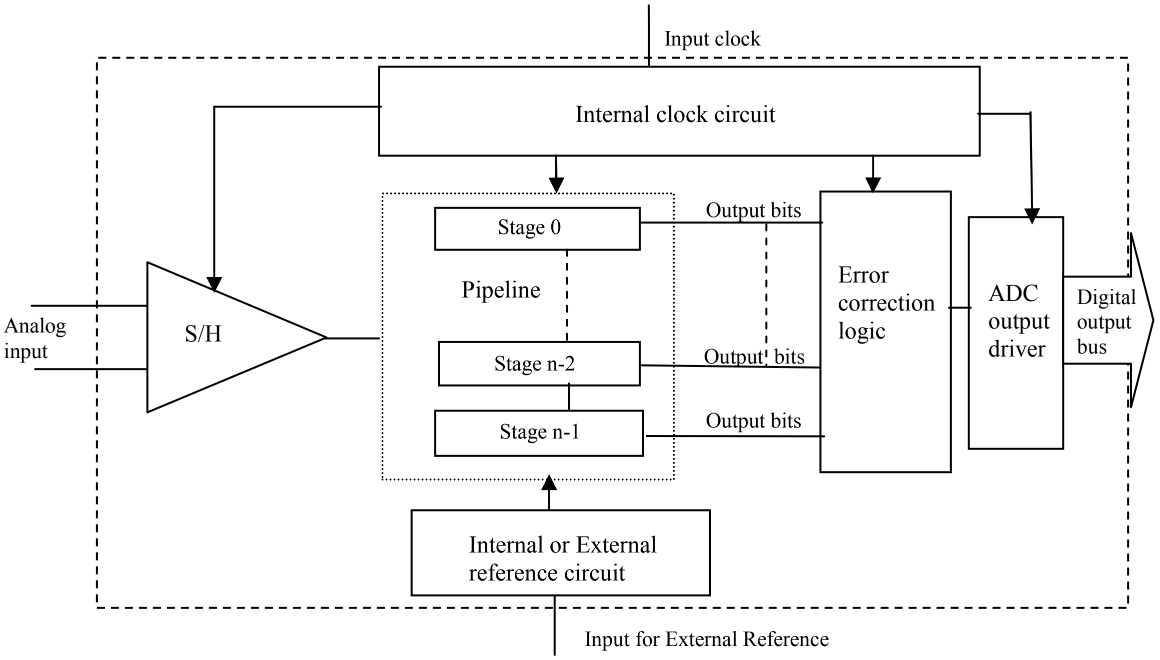

Fig. 1: High-Speed ADC Functional Block Diagram

For a high-speed and high-resolution ADC the pipeline architecture is the most popular consisting of multi-stages, each with a low resolution ADC, DAC and a sample-and-hold (S/H) amplifier. For example, the pipeline in the ADS5221 consists of ten stages: the first is a 3-bit quantizer, then there are eight middle stages with a 1.5-bit quantizer for each, and the final stage is a 4-bit flash. [1]

The basic operation of the ADC (Fig. 1, again) is that the input stage includes a high-bandwidth S/H amplifier accepting a single-ended or differential input signal, and the analog signal is captured at either the rising or falling edge of the sampling clock. Then the pipeline stages convert the analog signal to digital form, sequentially, with the most significant bit (MSB) first. The outputs from each pipeline stage are calculated with a correction algorithm in the digital error correction stage, where the final digital output of the ADC is produced. The digital output data is coded either in a straight offset binary, or a two’s complement format, and is output through the digital output driver. This conversion process results in a data latency of a few clock cycles. For example, the ADS5221 has 5 clock periods of the data latency.

The input stage impedance of the ADC is capacitive due to the input stray and sampling capacitors, effectively resulting in a dynamic impedance that is a function of the sampling and input frequencies. At a fixed sampling rate, increasing the signal frequency will decrease the input impedance and when it reaches about 100 MHz the ADC input impedance is down to a few hundred ohms in a common design. The analog input stage requires a common-mode voltage to act as a reference line around which the signal can swing, allowing it to be symmetrical while maintaining sufficient amplifier headroom to the supply rail. The common-mode voltage is typically half of the ADC supply voltage and it can be taken from the common-mode voltage pin provided on the ADC, or by an external dc voltage source.

In the reference circuitry of the ADC a bandgap is integrated to provide a high accuracy internal reference voltage for the ADC core. Bandgap references are generated by using the negative temperature coefficient of the base-emitter voltage and positive temperature coefficient of the thermal voltage and is independent of the supply voltage, the process and temperature. [2] With a bandgap, various accurate reference voltages can be generated using external capacitors. In the ADC it is also possible to provide circuitry to allow an external reference voltage to take over from the internal reference for more application flexibility, such as when multiple ADC gain matching is required; or if the full-scale input range is required, which is dependant on the amplitude of the reference voltage.

In the ADC clock section, an external clock is received from a sine wave or pulse source, with either a single-ended or differential input. The conversion rate of the ADC is determined by the input clock and it is converted into an internal clock for the internal circuits requires a duty cycle 50% ±5% in order to keep performance high. In some designs, such as the ADS5221, the ADC contains a duty cycle stabilizer (DCS) option which, when enabled, can allow a duty cycle between 30% and 70% without degrading the dynamic performance: the DCS adjusts the duty cycle to 50% with ±5% tolerance by correcting the non-sampling edge of the clock. With the DCS disabled a duty cycle variation more than ±5% will still degrade the device dynamic performance. Without DCS a duty cycle variation of more than ±5% requires reducing the sampling rate to a speed that can keep the S/H inside specifications, a mode suitable for non-uniform sampling ADC applications. In all cases, the incoming clock should have very low jitter to preserve high SNR. The ADC itself has very low aperture jitter (1 ps rms with current designs). The input clock is treated as analog on-chip and uses the analog supply rail, separated from the digital output driver supply, to limit digital noise.

An ADC is treated as an analog device in applications -- even though it is a mixed-signal device -- and, generally, the analog, digital, digital driver supplies are not tied together internally. Each of these supply pins must be bypassed separately with at least one 0.1 µF ceramic capacitor. The analog and digital supplies of the ADC may be tied together externally with a ferrite bead, or inductor, between the supply pins. [1][6] It is highly recommended that linear supplies, instead of switching types, should be used. Even with good filtering switching supplies can radiate noise that could interfere with any high-frequency input signal and cause unwanted modulation products. In CMOS designs the ADC can operate with a single +3.3 V supply or there is a separate supply pin for the output digital driver from 1.8 V to 3.3 V to offer flexible logic interface levels.

External Input Circuit For High-Speed ADCs

The ADC input structure is designed to accept both single-ended and differential analog signals. With differential, signals are applied to both inputs at the same amplitude, but with one 180° out-of-phase from the other. With single-ended, a signal is applied to only one input of the ADC while the other input is connected to the common-mode voltage. The amplitude of the differential signals at each input pin of the ADC are half that of the single-ended signal at the input pin. This allows more headroom for both ADC and the signal source stage. A differential driving can also minimize even-order harmonics to achieve the best ADC linearity performance and improves the noise immunity, based on the common-mode input rejection of the converter. Single-ended driving makes the ADC input operate with a larger voltage swing and can cause large even-order harmonics. A signal-ended input also limits the selection of the source op amp due to headroom requirements. For either differential or single-ended inputs a good input circuit should take into account the nature of both the signal source and the ADC input stage. From the signal source we should consider the signal frequency bandwidth, amplitude, amplitude and phase noise, and source impedance. For the IC input we should consider bandwidth, impedance, dynamic range and common-mode voltage. With different input signal conditions ADC dynamic performance changes and this is shown in following sections.

ADC input from transformer

One typical analog input configuration for high-speed ADCs is to use a transformer input circuit. The transformer has better harmonics in a wider frequency range compared with an op amp driver; Mini-Circuits' 1:2 turns ratio T4-6T RF transformer, for example, has a THD better than 85dB from 250 kHz to 250 MHz; some others can offer performance to 800 MHz. As a passive, a transformer does not add to the total noise, and it can step-up or step-down the signal amplitude for more flexibility, particularly reducing source signal level swing when a step-up transformer is used. The transformer also provides signal ac-coupling and conversion from single-ended to differential. When employed a transformer should not exhibit any core saturation at the ADC's full-scale input voltage level.

Figs. 2 and 3 show basic transformer input configurations with an ADS5221. [1][6] The ADC receives a differential ac signal (Fig. 2) from the RF transformer ADT1-1WT (1:1 turns ratio), and (in Fig. 3) it receives a single-ended ac signal from the same transformer. In both the transformer input signal is from a single-ended source impedance of 50 Ω. In order to match the source impedance, Rs, a source termination resistor, Rt, is required and it can be placed at input or output of the transformer. With low input frequencies an Rt of 50 Ω provides a good impedance match. When the input frequency is higher than about 100 MHz this would be a poor match. We noted that the analog input of the ADC requires a common-mode voltage as signal swing center providing the best symmetry -- and best performance -- for the signal and keeping sufficient amplifier headroom to the supply rail. A common-mode voltage, typically half the rail, is connected to the transformer center tap and it can be generated from a 3.3-V resistor divider (Fig. 2) or provided by the ADC itself from the common-mode pin. A real common-mode voltage may be shifted slightly from the design value (Figs. 2 and 3). To avoid possible instability small serial resistors, R1 and R2, are placed between the transformer and the ADC, and with the input capacitance they create a 1st-order low-pass filter (LPF) limiting high-frequency noise from the source. The cutoff frequency of this LPF can be changed by adding a small external capacitor, Cin, at the inputs. The resistor and capacitor values are typically in the range of 1 Ω to 100 , and 10 pF to 100 pF.

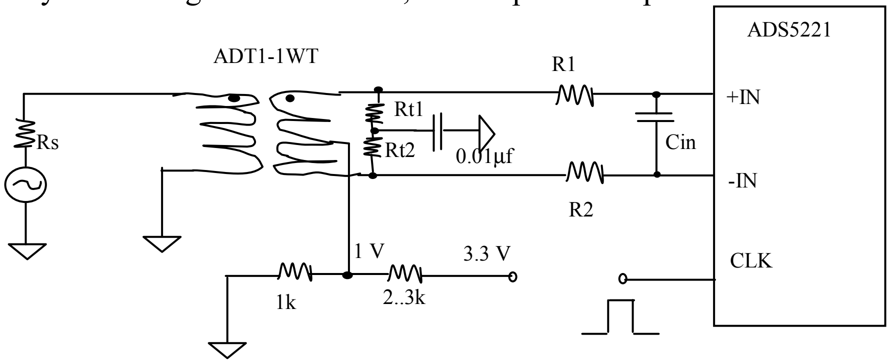

Fig. 2: Transformer-Coupled Differential Input (ADS5221 Wideband Application)

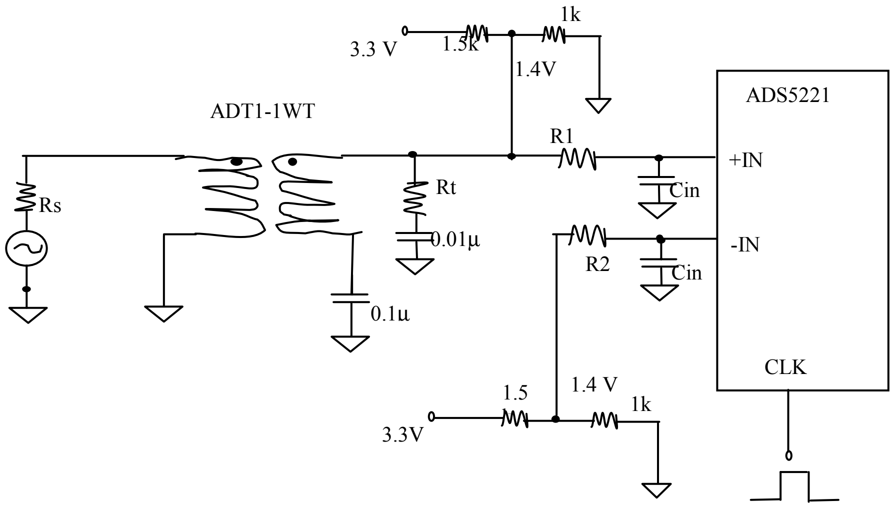

Fig. 3: Transformer-Coupled Single-Ended Input (ADS5221)

ADC Input From Operational Amplifier

Another typical analog input configuration of the high-speed ADC is op amp input circuit where dc signal coupling can be realized, which cannot be done with a transformer. The op amp can provide signal conditioning gain, level shifting, inversion, filtering, matching and power boosting. The single-ended and fully differential op amp can handle these tasks and they currently exist.

Figs. 4 and 5 are typical op amp circuits for high-speed ADCs. Fig. 4 shows a dc-coupled differential input through a THS4503 where the op amp gain is unity and the output common-mode voltage is 1.6 V, for narrowband applications, with the ADC, which is from VOCM, an input dc offset voltage of the op amp. A single-ended signal from the source is converted into differential by the op amp and then dc-coupled to the ADC. A small capacitor (eg 10 pF) in parallel with the feedback resistors of the op amp can be added to form a LPF to limit the bandwidth. The op amp is loaded with the input capacitance of the ADC introducing an additional pole in the signal path, decreasing the phase margin and threatening stability. A capacitive load greater than 2 pF can degrade the performance of some op amps [4] and to avoid possible instability small series resistors, R1 and R2, (from 10 Ω and 100 Ω) are placed between the output of the op amp and the input of the ADC. As with the transformer applications, a small capacitance, Cin, can be included to form a LPF. For the best frequency response the relationship between the op amp's noise gain, isolation resistors and ADC input capacitance should be considered. [4] An RLC network installed between op amp and ADC has been developed by TI's high-speed op amp group [3] to improve the combined SFDR.

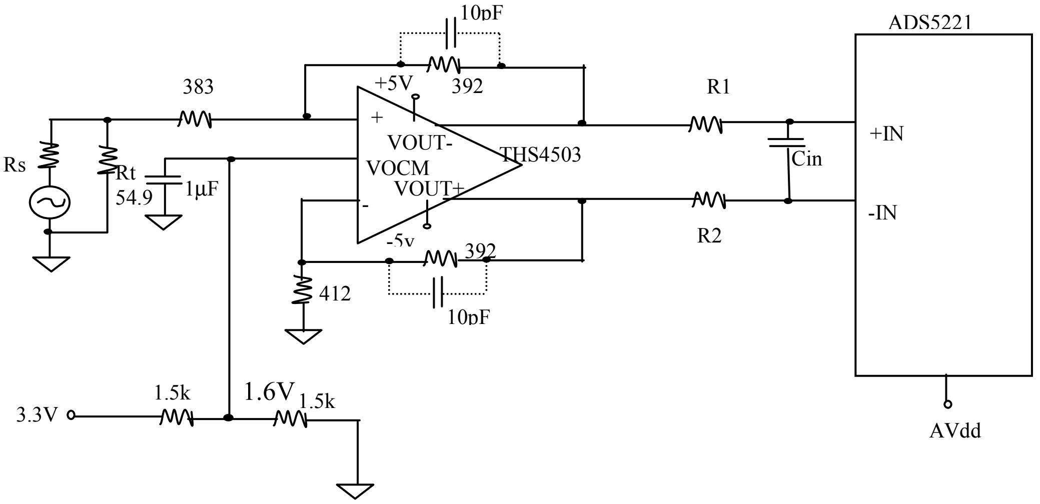

Fig. 4: Using Differential Amplifier (G = 1) To Dc-Couple ADC

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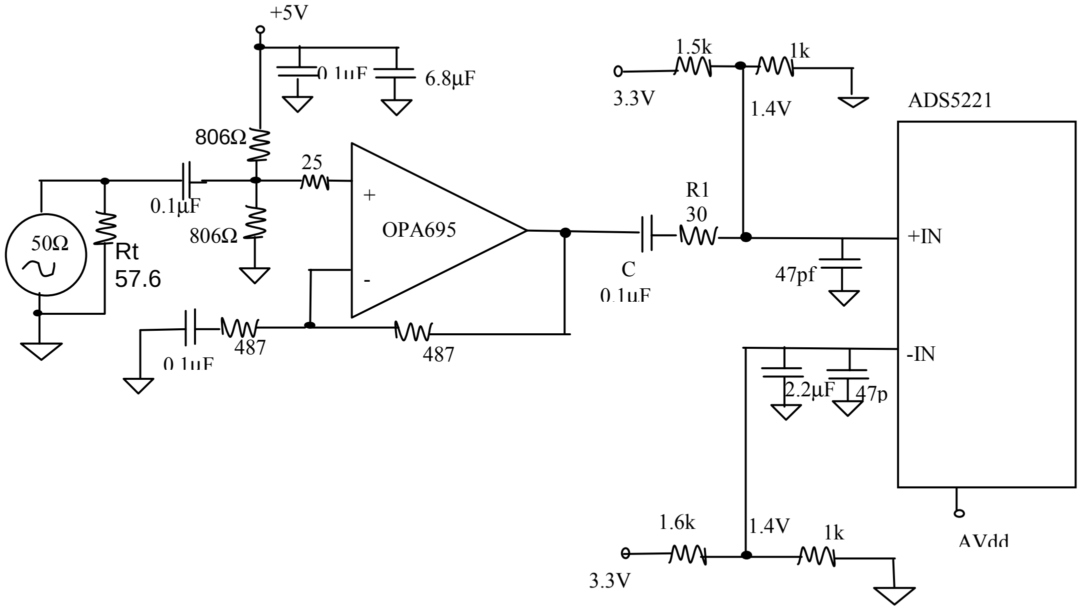

Fig. 5: Ac-Coupled Single-Ended Input of ADC Driven B Gain = 2 Op Amp

An ac-coupled single-ended input of an ADC (Fig. 5) is driven by an OPA695 [1][5] configured as a non-inverting amplifier with +5 V supply and an ac gain of 2. It is a current-feedback amplifier and good for both narrow and wideband applications. [4][5] The 2.5-V dc offset of the amplifier is separated from the 1.4-V common-mode voltage by blocking capacitor, C. The ADC receives a single-ended input signal at one input pin and the other is connected to the common-mode voltage. Rt is the signal source termination resistor and R1 is the stability resistor for load capacitance.

Test Data

With different input configurations the ADC performance is different. In general, circuit component values can be adjusted to reach the best ADC performance. The input frequency range, SNR and SFDR of the ADC can be increased by adjusting the input network components. For example, adjusting serial and termination resistors, the input capacitance, Cin, and the common-mode voltage SNR can be changed as much as 3 dB, and SFDR can be changed as much as 10 dB with different input frequencies and input configurations. The measurements show that SFDR and THD are more sensitive to circuit component values in the single-ended input configuration because the ADC is operating with a larger input amplitude. In both configurations SNR and SFDR can be improved by decreasing the ADC driver supply voltage from 3.3 V to 2.5 V. This is shown in the following tables

- Table 1 compares FFT performance in differential and single-ended transformer input circuits at 65 Msample/s. The differential transformer input circuit provides a few dB better SFDR below Nyquist. SNR from both differential and single-end transformer input circuits are almost the same below Nyquist, but above Nyquist the differential input circuit provides much better FFT performance.
- Table 2 compares FFT performance of differential transformer and differential op amp inputs. The differential transformer input configuration provides good SNR and SFDR at a much wider frequency than differential op amps because of op amp limitations. For example, below 20 MHz, the op amp didn't degrade the ADC performance, but at input frequencies above 20 MHz the performance of the ADC degrades significantly due to bandwidth limitations. In the op amp input serial resistors, R1 and R2, and Cin should be adjusted for the best ADC performance.
- Table 3 compares FFT performance of the ADC with different input common-mode voltages; sometimes the best is not the design value due to design and process shortages. The test shows that the best common-mode voltage is about 1 V (resistor divider, Fig. 2). Testing four ICs shows that with 1.5-V common-mode voltage the SFDR and THD dip around the Nyquist frequency. With 1 V ±0.1 V input common-mode voltage the SFDR and THD appear flat around Nyquist. There is a 1 dB to 8 dB difference in SFDR and THD with common-mode voltages at 1.5 V or 1 V. The Vcm is measured at the analog input pins with no clock signal applied and it is from the simple resistor divider (Fig. 1). In Figs. 2 and 4 the Vcm from the resistor divider is 1.4 V (no clock) for a single-ended input configuration. In Fig. 3 the Vcm from the op amp is about 1.5 V, which is for narrowband op amp differential input configuration.

Table 1: FFT of ADS5221 with differential or single-ended (SE) signal from transformer input circuits at clock of 65 Msample/s

Input frequency (MHz)	SNR (dBFS)		SFDR (dBFS)		THD (dBFS)	
	Differential,	SE	Differential,	SE	Differential,	SE
2	70	70	89	82	87	81
10	70	70	87	84	86	81
20	69.5	69.2	84	75	82	74
32	68.2		87		81	
40	68		85		80	
50	67		83		80	
60	67		82		79.5	

Table 2: FFT of ADS5221from differential transformer input or OPA (THS4503) differential input at clock 65 Msample/s

Input frequency (MHz)	SNR (dBFS)		SFDR (dBFS)		THD (dBFS)	
	Transformer,	OPA	Transformer	OPA	Transformer,	OPA
2	70	69.5	89	90	87	89
10	70	69.3	87	88	86	84
15	69.8	69.1	85	87	83	84
20	69.5	69	84	78	82	77

Table 3: SFDR of ADS5221 with differential transformer input vs different common-mode voltage at clock 65 Msample/s

	Vcm = 1.5 V	Vcm = 1 V ± 0.1 V
Input Freq (MHz)	SFDR (dBFS)	SFDR (dBFS)
2.5	88	89
9.7	89	89
20.0	83	84
32.0	82	86
40.0	85	85
50.0	84	84
60.0	82	82

Conclusions

The dynamic performance of a high-speed ADC is sensitive to the external input circuit because of its switch-capacitor input stage and wide frequency range, as well as high sampling speed. Differential input provides better ADC dynamic performance, in general, including SFDR, THD and input frequency range compared to single-ended inputs. The ADC performance is less sensitive to the external circuit components using differential inputs. Compared with op amp inputs the transformer input provides slightly better SNR at capable op amp frequencies, and much better SNR and SFDR at high frequencies. The op amp input contributes high harmonics and noise to ADC performance at those frequencies because of bandwidth limitations of the op amp. ADC performance with op amp inputs is more sensitive to the serial resistors between ADC and OPA than it is with transformer inputs. However, op amp inputs have flexible signal conditioning and dc-coupling capable of power gain and larger voltage swings to the ADC. At low input frequencies (less than 20 MHz for the THS4503) the op amp input provides compatible ADC performance compared with a transformer input. In both differential and single-ended inputs the common-mode voltage is important to ADC performance and can make significant changes in performance. The high-speed ADC external input circuit can be simple but each component can affect the ADC performance to some degree or other.

References

[1] ADS5221 data sheet, SBAS262A, Revised December 2003
[2] Mikael Gustavsson, 2000, COMS Data Converters For Communications, Kluwer Academic Publishers
[3] THS4503 data sheet, SLOS352B, Revised August 2002
[4] OPA690 data sheet, SBOS223A, Revised July 2002
[5] OPA695 data sheet, SBOS256, August 2002
[6] ADS5221 EVM user guide, SBAU094, in process

Biography

Hui-Qing Liu is an applications engineer for TI’s high-speed ADC product group, and technically supports various high-speed ADC applications. She has many years of experience in the applications of AFE (analog front end), op amps, DSP, microcontrollers and image processing. Hui-Qing earned a BS degree from Harbin Institute of Technology (PRC) and an MS degree from the University of Arizona.

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