

## Basic Guidelines For Using Analog-To-Digital Converters

by Gary Hendrickson, Intersil Corporation

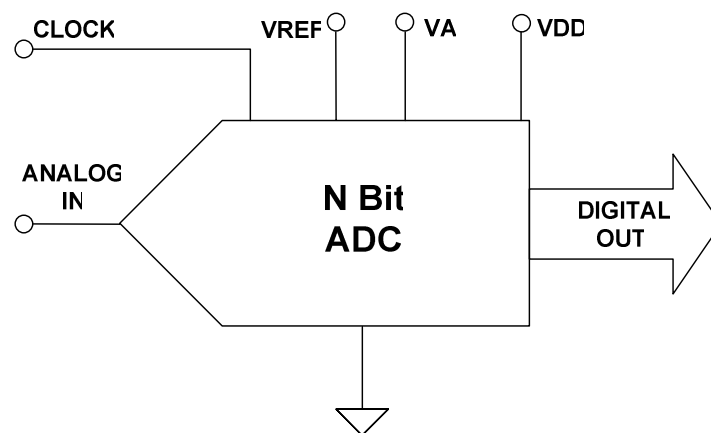
Analog-to-digital converters (ADCs, also sometimes called *data converters* or simply *converters*) change real-world analog signals such as sound, temperature, pressure and light to digital signals that can be processed in the digital domain. Analog design engineers like to say "The world is analog," but most signal processing is done by digital computers today -- the days of analog computers are over.

ADCs are found in such a large number of applications that they are almost a commodity. Historically, converters were components requiring specialized knowledge to design and manufacture, resulting in expensive solutions. A 12-bit/500-kHz ADC sold for about \$270 in 1975. Modern converters have come down in price dramatically over the years, capitalizing on the same technology advances as digital integrated circuits (ICs). That same 12-bit/500-kHz function is available today for less than a dollar. ADCs are commonly used in communications, instrumentation & measurement, and computer systems where they can facilitate digital signal processing and/or storage of information. Often the ADC function is integrated along with digital circuitry on the same chip, but there are also applications where performance requirements dictate that a stand-alone ADC must be used. In cell phones the ADC function has been integrated into the digital chip, while the cellular basestation (with its higher requirements) relies on separate stand-alone ADCs which can deliver the ultimate in performance.

ADCs have the following characteristics:

- Analog Input(s): both single channel and multiple channels are available
- Reference Input: this voltage can be supplied externally, or may be inside the ADC
- Clock Input: typically external, this determines the conversion rate of the ADC
- Power Supply Input(s): often there are both analog and digital supply pins
- Digital Output: ADCs can have parallel or serial digital outputs

Fig. 1 shows the block diagram of a typical ADC.



**Fig. 1: Analog-To-Digital Converter (ADC) Block Diagram**

While ADCs may appear to be simple, they must be used correctly to achieve optimum performance and exhibit some of the same performance limitations as simple analog amplifiers: finite gain; offset voltages; common-mode input voltages; and harmonic distortion, to name a few. The sampling nature of an ADC introduces additional considerations of clock jitter and aliasing. The following will help you to realize the full performance of an ADC in a design.

## Analog Input

Careful attention must be paid to keeping the analog signal to the ADC as clean as possible: *garbage-in* typically results in *digitized-garbage out*. The analog signal path should be kept clear of any fast switching digital signal lines that may couple into the analog path. While the simplified block diagram shows a single-ended analog input, differential analog inputs have become more common on high-performance ADCs. Driving an ADC differentially will provide greater common-mode noise rejection and typically will allow for better ac performance due to smaller on-chip signal swings. Differential drive is typically accomplished using a differential amplifier, or transformer. A transformer usually will provide better performance than an amplifier because the active amplifier is an additional source of noise, which will affect overall performance. However, transformers are not a viable solution when you need to process signals with dc information, due to their inherent dc-blocking characteristics. The driving amplifier's noise and linearity performance must be considered when designing the pre-drive circuitry. Note that since high-performance ADCs often have very high input bandwidth, filtering directly at the ADC's input pins will reduce the amount of wideband noise being aliased down to the baseband.

## Reference Input

The reference input should be treated as another analog input and kept clean as possible: any noise on the reference voltage ( $V_{REF}$ ) is indistinguishable from noise on the analog signal. Typically the ADC data sheet will specify the required decoupling capacitors. These capacitors should be placed as close to the ADC as possible. PCB designers will sometimes place decoupling capacitors on the backside of the PCB to conserve board space -- this should be avoided if possible, since the inductance of the vias will reduce the capacitor's effectiveness at high frequencies.  $V_{REF}$  usually sets the full-scale input range of the ADC, so reducing the value of the  $V_{REF}$  voltage will reduce the LSB value of the ADC, making the ADC more sensitive to noise in the system. (A 1-V full-scale 10-bit ADC has an LSB value equal to  $1\text{ V}/2^{10} = \sim 1\text{ mV}$ .)

## Clock Input

Depending on the application, the digital clock input may be just as critical as the analog inputs. There are two major sources of noise in the ADC: one due to the quantization of the input signal (proportional to the number of bits in the ADC), the other due to clock jitter (sampling the input at the wrong time). Quantization noise limits the maximum possible SNR in a non-oversampled ADC application according to the formula:

$$SNR = 6.02N + 1.76dB$$

(N=Number of Bits, SNR=Signal-to-Noise Ratio)

Intuitively, this makes sense: every time you add a bit you double the total number of ADC codes and cut the quantization uncertainty in half (6 dB). A 10-bit ADC is therefore theoretically capable of providing 61.96 dB SNR. Any jitter on the sampling clock will reduce this further according to the following equation:

$$SNR_j = 20 \log \left[ \frac{1}{2\pi f_a t_j} \right]$$

where,  $SNR_j$  is the jitter-limited SNR,  $f_a$  is the analog input frequency, and  $t_j$  is the rms clock jitter.

A sampling clock with jitter equal to 8 ps digitizing a 70-MHz analog signal results in a jitter-limited SNR of approximately 49 dB, effectively reducing the effectiveness of a 10-bit ADC to about 8 bit. The clock jitter must be  $<2$  ps to achieve an SNR equivalent to 10 bit. There are many other second-order contributors to SNR, but the above equations are a good first-order approximation. Differential clocking is often used to reduce jitter.

## Power Supply Input

Most ADCs have separate power supply inputs, one for the analog circuits and one for the digital. Adequate decoupling capacitors, located as close to the ADC as possible, are recommended. Minimize the use of PCB vias and the trace length from the ADC power pin to the decoupling capacitor to keep inductance between the ADC and the capacitor to a minimum. As with reference voltage decoupling, board designers sometimes place decoupling capacitors on the back side of the PCB under a chip to conserve board space -- this should be avoided for the same reasons. The ADC's data sheet usually shows the recommended decoupling scheme. Dedicated PCB planes for both supply and ground voltages are often necessary to achieve the specified performance.

## Digital Outputs

An ADC's switching digital outputs can generate noise transients that can couple back to the sensitive analog portion of the ADC, causing errors. Reducing the capacitive load that the ADC drives by minimizing the output trace lengths can help here, as well as placing series resistors right at the ADC outputs to reduce the output current spikes. The ADC's data sheet usually has a recommendation.

## About The Author

Gary Hendrickson is a staff applications engineer for Intersil's Analog & Mixed-Signal products group. Prior to Intersil, Gary spent 15 years working as a design engineer at IBM in their Microelectronics division. He also worked for 8 years as an applications engineer at Analog Devices in their High-Speed Converter group. Gary earned a BSEE degree from Rutgers University and an MSEE from Syracuse University.

