

## **Understand the Limits of Your ADC Input Circuit Before Starting Conversions**

*by Miroslav Oljaca*

*Data Acquisition Products, Texas Instruments Incorporated*

High-performance analog application designs that implement ADCs require a detailed understanding of the components used as well as the interactions within the system. The analog input of a successive-approximation register (SAR) ADC interacts with the circuitry that drives it and can present an unknown load. Data sheet specifications may mislead the user into thinking that analog inputs, for example, are linear and carry a static load when, in fact they are dynamic and require specially-designed buffer circuitry. This article looks at the architecture of modern SAR ADCs, and examines the conversion process in detail. The analysis reveals the considerations needed for designing circuitry to drive these ADCs with optimal results.

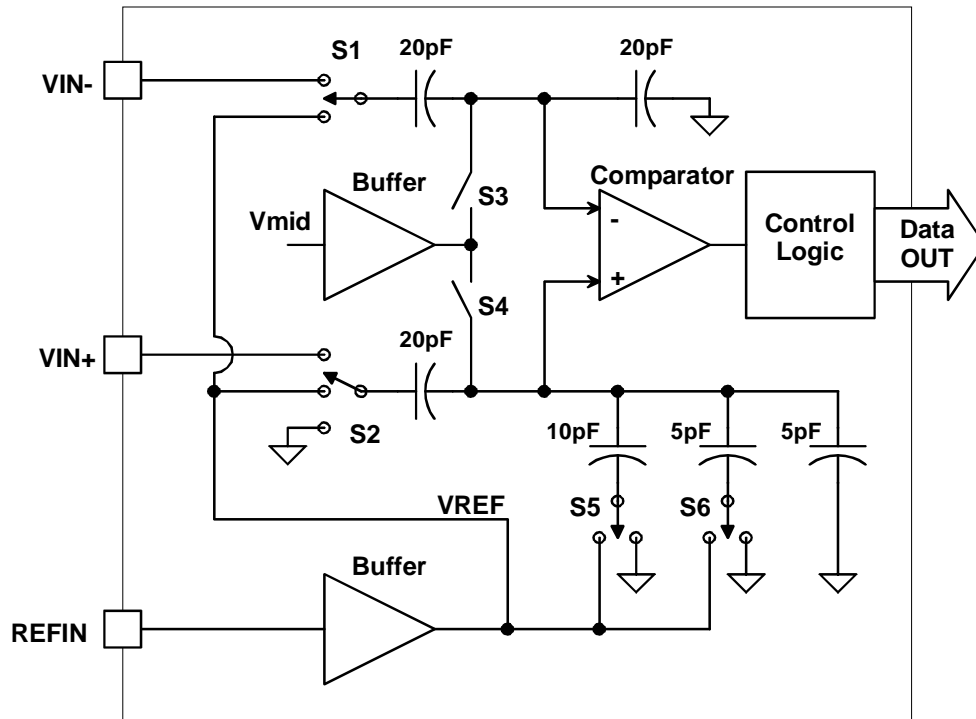
### **Introduction**

In high-performance analog applications that include an analog-to-digital converter, the overall system accuracy does not depend only on the quality of ADC. Measurement results will be directly proportional to the signal that is present at the analog input of the converter at the moment of sampling-to-conversion transition. The voltage that is present on the analog input at that moment will be "frozen" on the converter's sampling capacitor. Consequently, the result of the conversion will be directly proportional to that voltage. If the signal on the analog input of the converter is distorted, the conversion results will be distorted as well. Measuring the quality of the signal on the ADC input provides designers with an idea of the accuracy limits of the system. Understanding the internal structure and component nonlinearity can help to overcome these physical "limits."

### **SAR ADC Structure**

This study used the high-performance ADS8361 SAR ADC (a Burr-Brown product from Texas Instruments). For our analyses we assume that the most significant bit (MSB) capacitor has a value of 20 pF. The capacitor following the MSB capacitor will have half that value, or 10 pF. In the example of Fig. 1 we have a three-bit converter; thus, the least significant bit (LSB) capacitor will have one-quarter of the MSB capacitor value, or 5 pF. To make an ideal conversion, a termination capacitor having the same value as the LSB capacitor is added. The effect of this added capacitor is that the sum of all the capacitors below the MSB becomes 20 pF, the same as the MSB.

This structure is for the ADS8361 and similar bipolar input parts. Others may be similar but not identical.



**Fig. 1: Representative Block Diagram Of SAR Input Stage**

The positive analog input,  $V_{IN+}$ , is sampled by the MSB capacitor through switch S2 and the capacitive conversion network composed of three capacitors and two switches, S5 and S6. The negative analog input,  $V_{IN-}$ , is sampled by two MSB-valued capacitors in series through switch S1. These two analog inputs, positive and negative, permit this ADC to sample differential signals, a key factor in this analysis.

The reference voltage applied to the REFIN input, and buffered internally is distributed to all the switches. Switches S3 and S4 are connected to the buffered  $V_{mid}$  voltage, whose value is about 2.4 V with a 5-V supply and varies in direct proportion to the supply. This buffer is important for proper charge distribution during the sampling period.

The comparator input signals are connected in parallel to switches S3 and S4. During conversion the comparator output will be processed by the control logic, which will set up the switches S2, S5 and S6 properly.

### SAR ADC Sampling Process

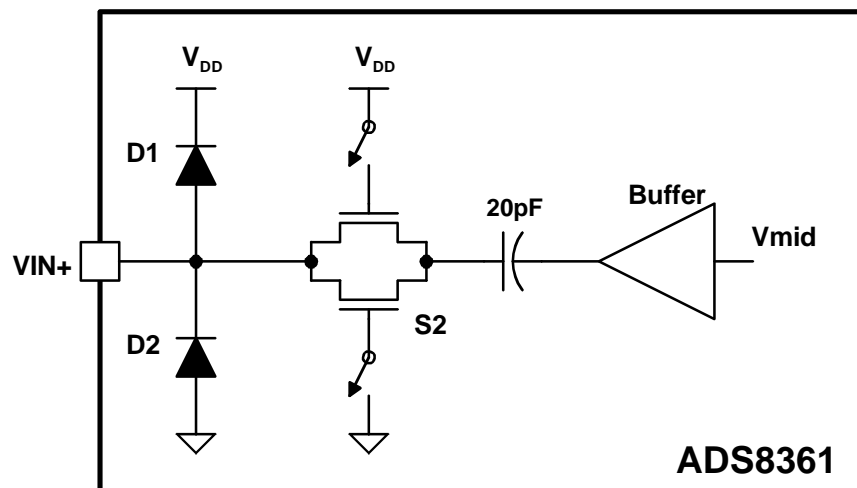
At the end of the conversion the ADS8361 will automatically go into the sampling state. The positions of switches S5 and S6 in the capacitive conversion network are unknown, as is the position of switch S2, which can be closed to either ground or the reference voltage. The switch status depends on the conversion results. We know for certain that at this point in time switch S1 is connected to the reference voltage. The sampling process

will initiate closing switches S3 and S4. Closing these switches shorts the inputs of the comparator and connects them to  $V_{mid}$ .

As the positions of switches S5 and S6 are unknown, the equivalent capacitance of the network is also unknown. For proper sampling, the capacitive conversion network must have an equivalent capacitance that is equal to the MSB capacitor. To obtain that capacitance, switches S5 and S6 in this step connect the associated capacitors to the ground terminal.

Up to now all changes are made internally in the ADS8361 and the analog input signals are not affected. In the next step, input switches S1 and S2 will close, and the input signal will be sampled on the input MSB capacitors. This period is the most critical period for the input buffer. To have accurate results from the conversion, the input buffer must be able to charge the sampling MSB capacitors to the proper voltage value during sampling.

The input structure of the positive input can be described in the following way: The input pin is directly connected to two ESD protection diodes (see Fig. 2) directly connected to the rail and ground, protecting the input circuitry from accidental damage. During normal operation, when the input signal is between the rails of the supply, these diodes act only as parasitic capacitors. The "ideal" sampling switch is now replaced with two FETs which are ON when the input signal is sampled, connecting the sampling capacitor and the rest of the circuit to the input signal. During the data conversion process, these FETs are OFF, disconnecting the input signal from the sampling capacitor.



**Fig. 2: Equivalent Circuit Of The Signal Input**

### ADC Analog Input

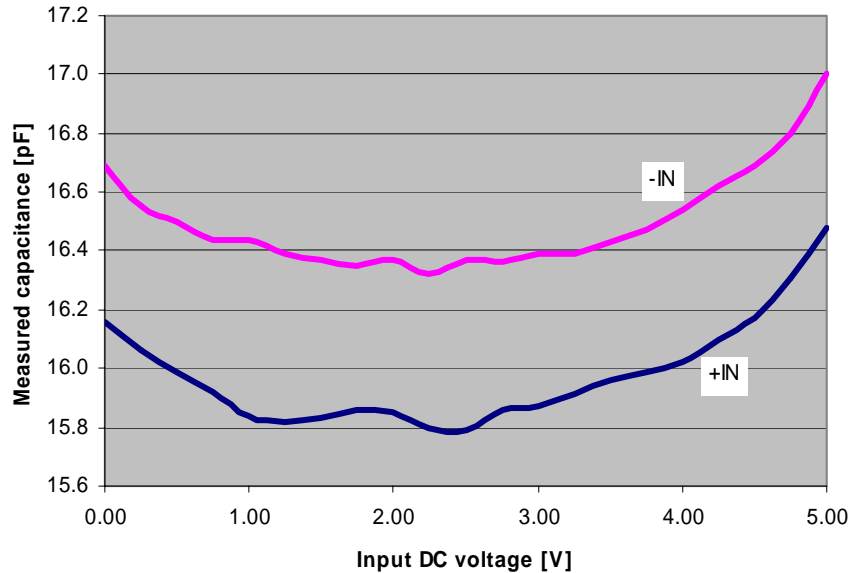
Understanding the input of the ADC drives the design of an input buffer. The ESD protection diodes, during normal operation, have no significant influence on the input signal. Compared to the rest of the circuit, their parasitic capacitance is small and can be disregarded and an input buffer has no problem in properly driving a load equivalent to

these two diodes. On the other hand, the input sampling capacitor, together with the input FETs, and an internal buffer, presents a load that has great influence on an input buffer. To understand the influence of different parameters, a series of tests were done.

### Equivalent Input Capacitance

The first test measured the equivalent input capacitance of the positive and negative analog inputs into the ADC. A 1-MHz signal of 20 mVp-p was applied at different dc levels. This small ac signal was applied so that the ESD input diodes would not start to conduct when the dc signal was close to the power rails. The first measurement was made with the ADC in the conversion state, or with input FETs in the OFF state.

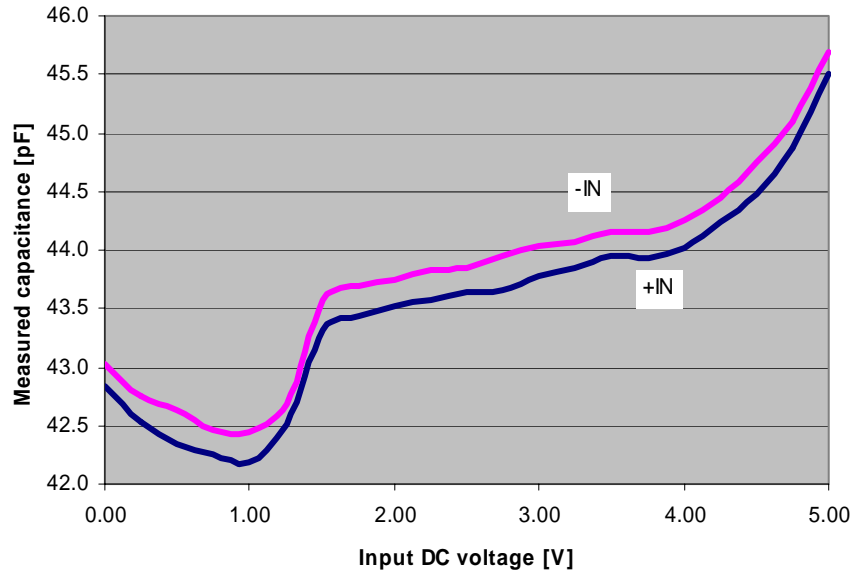
The measured equivalent input capacitance also includes the test PCB stray capacitance and Fig. 3 presents the measured results.



**Fig. 3: Equivalent Input Capacitance of ADS8361 in Conversion Mode**

We can see that the equivalent capacitance is quite constant over the full input range and does not present any particular challenge for an input buffer.

The next measurement was made with the same set-up, but with the ADC in the sampling mode, with the input FETs ON, and the internal sampling capacitor connected to the applied signal. The measured results are shown in Fig. 4.



**Fig. 4: Equivalent Input Capacitance of ADS8361 in Sampling Mode**

This measurement shows that for an applied dc voltage between 1.25 V and 3.75 V, the equivalent input capacitance is quite constant but, for an applied dc voltage between 0 V and 1.25 V, and between 3.75 V to 5 V, there is significant change.

### **Influence of the Input Switch FETs**

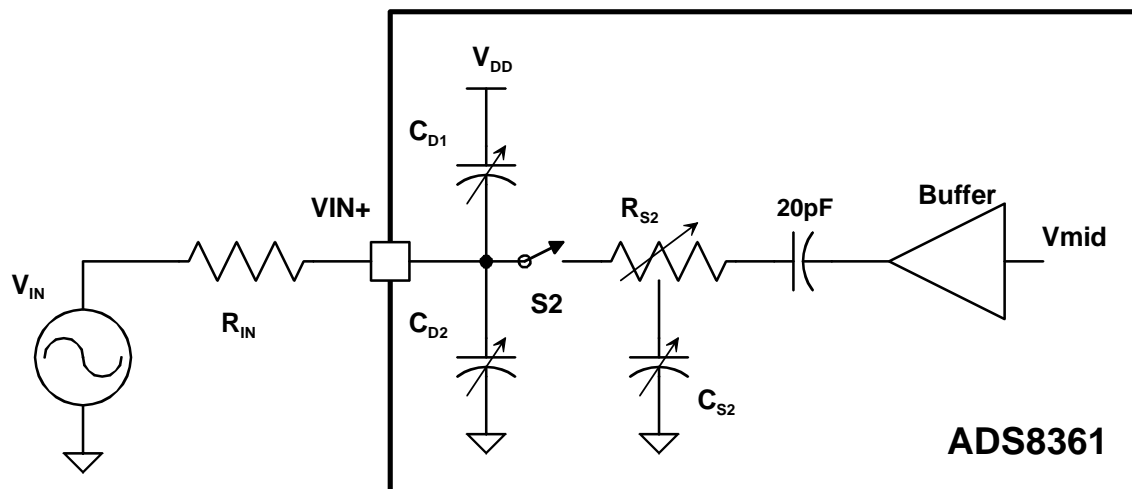
To understand this phenomenon, we need to understand how measurements are made. Calculation of the equivalent capacitance is obtained measuring the angle between the voltage and the current of the DUT. This angle is influenced by the equivalent resistance and the equivalent capacitance of the circuit in question. If there is any change in the equivalent resistance of the circuit, it can be presented as a change in capacitance.

For proper operation, the input switch FETs require the gate-source voltage to be greater than 1 V. Between 1.25 V and 3.75 V, both input FETs are ON, and the equivalent resistance has a minimum value. As the voltage approaches the end of this range, one of the FET transistors will start to transition from ON to OFF. This causes a change in the equivalent resistance as well the capacitance. This nonlinear load presents one of the major challenges for an input buffer to provide a proper signal to the ADC analog input.

## Nonlinear Load of the ADC Input

The conversion results depend on the performance of the input buffer as well as the ADC. The easiest way to evaluate system accuracy limits is to measure the quality of the signal on the ADC input. An examination of the signal distortion, caused by a combination of the input buffer circuit and the equivalent nonlinear load of the ADC analog signal input, can answer several questions and help make design easier.

The input sampling switch from Fig. 2 as well as the ESD protection diodes can be presented with their parasitic components. In Fig. 5 diodes D1 and D2 are replaced with nonlinear capacitors,  $C_{D1}$  and  $C_{D2}$ , whose values are voltage-dependent changing with the input signal level. The input FETs are replaced with an ideal switch, S2, and a variable resistor  $R_{S2}$ , as well as a distributed capacitor  $C_{S2}$ , which are both also voltage-dependent.



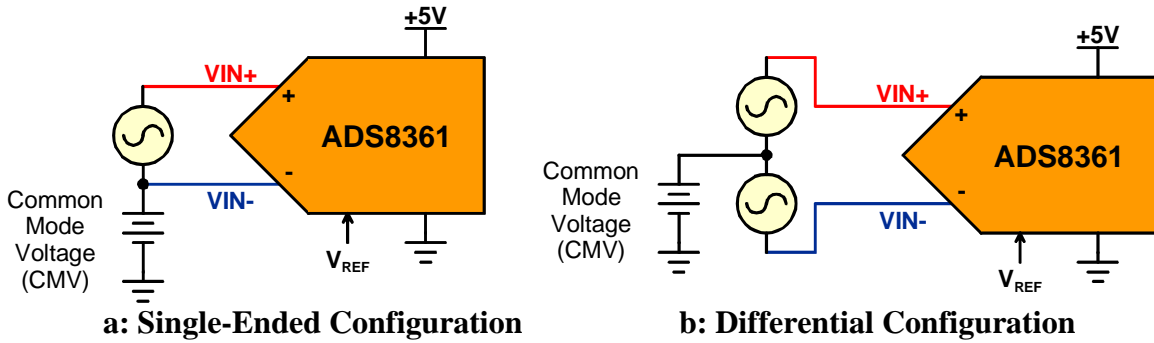
**Fig. 5: Equivalent Non-Linear Load of ADC's Input**

The equivalent input circuit (Fig.5, again) can explain the measurement results in Figs. 3 and 4. When S2 is open, the equivalent capacitance of the input is a parallel combination of capacitors  $C_{D1}$  and  $C_{D2}$  and the slight change in capacitance (Fig. 3) is caused by their voltage coefficient. When S2 is closed, the input capacitance starts to be a combination of  $C_{S2}$  and  $R_{S2}$ , as well as  $C_{D1}$  and  $C_{D2}$ . As shown before, the input FETs are linear when gate-source voltage is greater than 1 V, but when this voltage drops below 1 V, the equivalent FET resistance changes, together with the parasitic capacitance. This explains why the equivalent input capacitance (Fig. 4) is only linear from 1.25 V to 3.75 V.

## Input Signals of the SAR ADC Converter

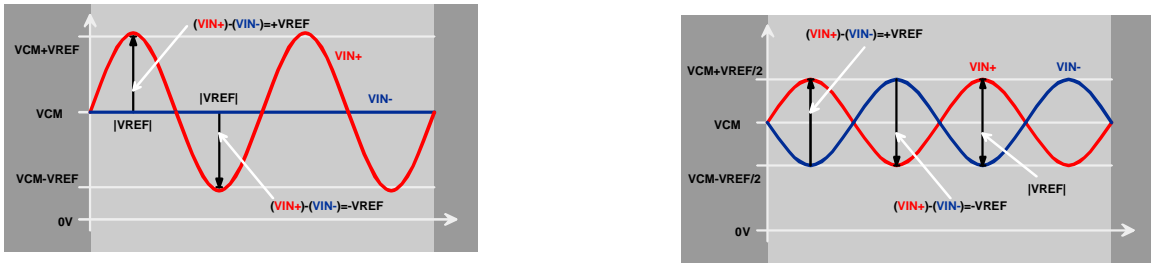
Most of the advanced SAR ADCs are designed for industrial applications and are able to accept two signal types. The first is single-ended, and the second is differential. When a single-ended signal is measured, the negative input is connected to the common-mode voltage and the measured signal is applied to the positive analog input of the ADC (Fig.

6a). In differential measurements (Fig. 6b) both signals are connected to the negative and positive inputs, and they are offset for the common-mode voltage.



**Fig. 6: Measurement of Single-Ended and Differential Signals**

When the ADC is used with a 2.5-V reference voltage, in a single-ended configuration, the negative input will be connected to the same reference voltage, and the positive analog input will swing between 0 V and 5 V. The full-scale voltage will be  $(VIN+) - (VIN-) = \pm 2.5$  V (Fig. 7a). With differential the signals on both inputs will be offset for the common-mode voltage and will swing  $\pm 1.25$  V (Fig. 7b). As they are  $180^\circ$  out-of-phase, the full-scale voltage for the differential signal will be  $(VIN+) - (VIN-) = \pm 2.5$  V.



**a: Single-Ended Waveform**

**b: Differential Waveform**

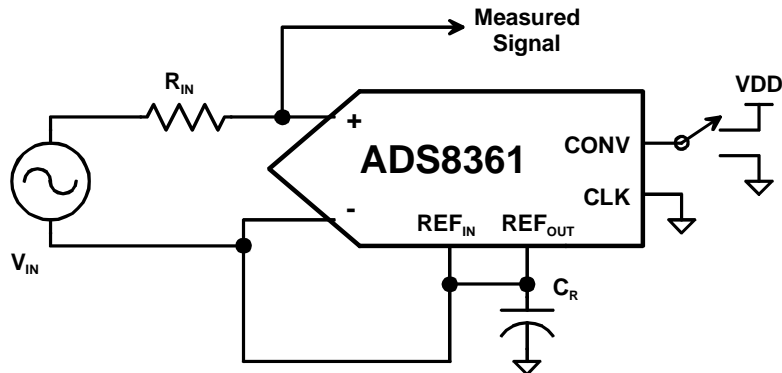
**Fig. 7: Waveforms of Measured Single-Ended and Differential signals**

## Measurement Results

As explained the input of the ADC is a nonlinear load which will interact with the analog signal source, or the input analog front end buffer, and distort the input signal. Also, op amps used as input buffers are not ideal circuits, their output driving performances influencing system characteristics. To understand the limits of the system, a high-quality analog signal was applied to the input of the buffer. The corresponding analog inputs were put into sampling or conversion mode, measuring the quality of the analog signal at the same time. During these measurements, the ADC did not convert the applied signal.

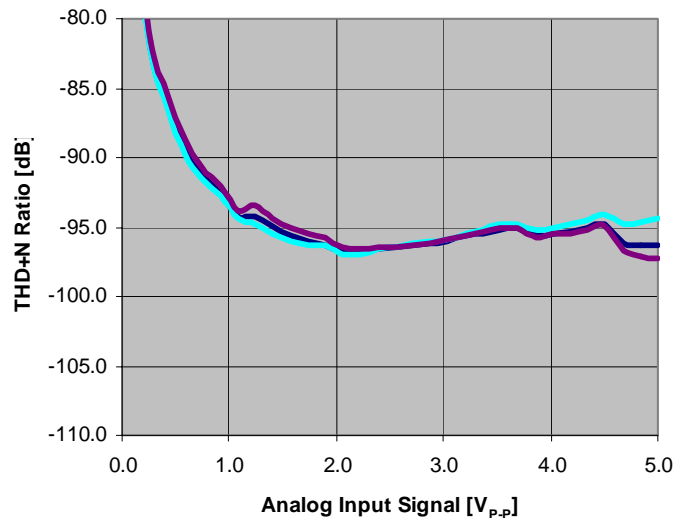
## Measurement of the Single-Ended Signal

The measurement configuration (Fig. 8) is used to evaluate the interaction between the input buffer and the ADC input, when a single-ended signal is measured. The CLK signal is tied to ground; the CONV signal is switched between VDD and ground. The CONV signal will change the state of the input analog switch from that in Fig. 2. In this way, it will be possible to evaluate the influence of the ADC nonlinear load.



**Fig. 8: Measurement of Single-Ended Input**

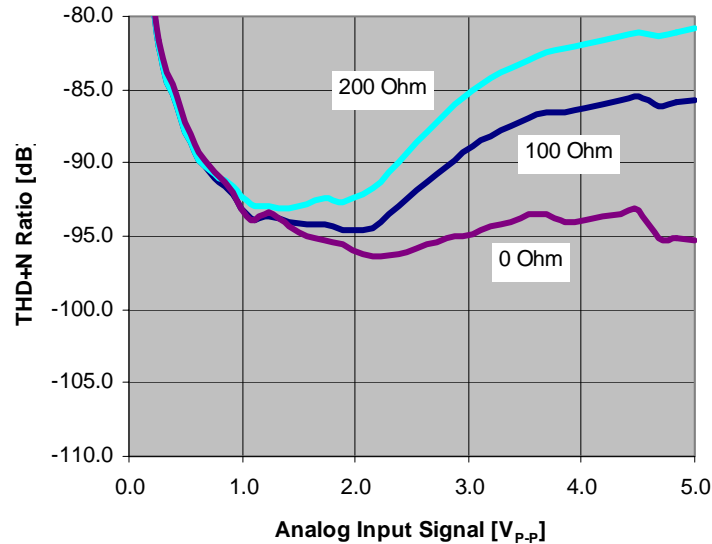
With the voltage source driving the ADC through  $R_{IN}$ , a separate instrument measured the positive input voltage, first at a fixed frequency of 100 kHz, changing the input from 0.1 V<sub>p-p</sub> up to 5 V<sub>p-p</sub>. THD+N was measured after  $R_{IN}$ , at the ADC input, for three different values of input resistor, 0  $\Omega$ , 100  $\Omega$  and 200  $\Omega$ . The measurement results for the ADC in conversion mode (when the analog input switch is open) are shown in Fig. 9.



**Fig. 9: Distortion On ADC Input Pin In Conversion Mode**

Noise will be dominant for a small input signal which explains the poor measurements for signals smaller than 1 V<sub>p-p</sub>. Changes for different resistance values are small.

For the second group of measurements, the ADC was put into sampling mode, and the input FETs changed from OFF to ON. Again, the input frequency was fixed at 100 kHz and the input swung between 0.1 V<sub>p-p</sub> and 5 V<sub>p-p</sub>. THD+N was, again, measured after R<sub>IN</sub> and shows (Fig. 10) the real nature of the dc nonlinear input load.

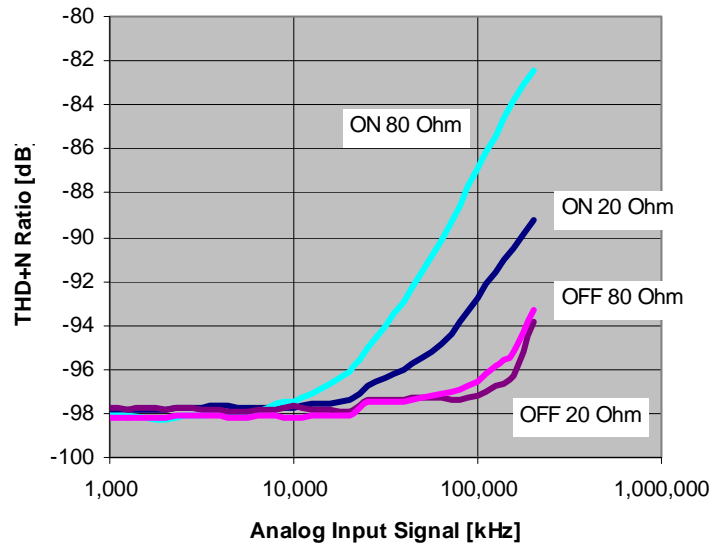


**Fig. 10: Distortion on ADC Input Pin In Sampling Mode**

As in previous measurements noise is dominant with small input voltages but when the input FETs are ON, the nonlinear load starts to interact with the input resistor, which represents the equivalent output resistance of the input. From the measurements, we can see that as the input resistance increases, for input signals greater than 2 V<sub>p-p</sub>, the THD becomes worse. With the 200-Ω input resistor and 5 V<sub>p-p</sub> input we can expect to lose up to 15dB.

One good design practice to overcome this problem is to use fast operational amplifiers with low output resistance. In this way the input buffer will force good input signals into the ADC. Unfortunately, this can lead to a stability problem of the system, as well as additional unwanted noise.

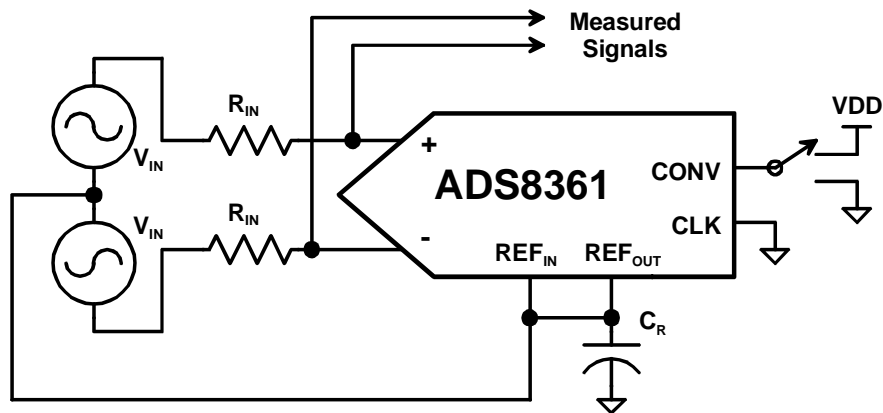
The typical output impedance of high-precision operational amplifiers is in the range from 30 Ω to 100 Ω. The previous measurements were made with an input signal at 100 kHz. As the nonlinear input load is a combination of the resistors and capacitors, it is frequency-dependent and additional measurements were made with a single-ended signal of 5 V<sub>p-p</sub> with the signal frequency varying from 1 kHz up to 200 kHz. Results for both sampling and conversion modes are presented in Fig. 11 for input resistances of 20 Ω and 80 Ω. Measurement results show that for an input signal frequency less than 10 kHz, there is no change in the performance for the input resistance variation.



**Fig. 11: Frequency Distortion Over Frequency In Sampling Mode**

### Measurement of the Differential Signal

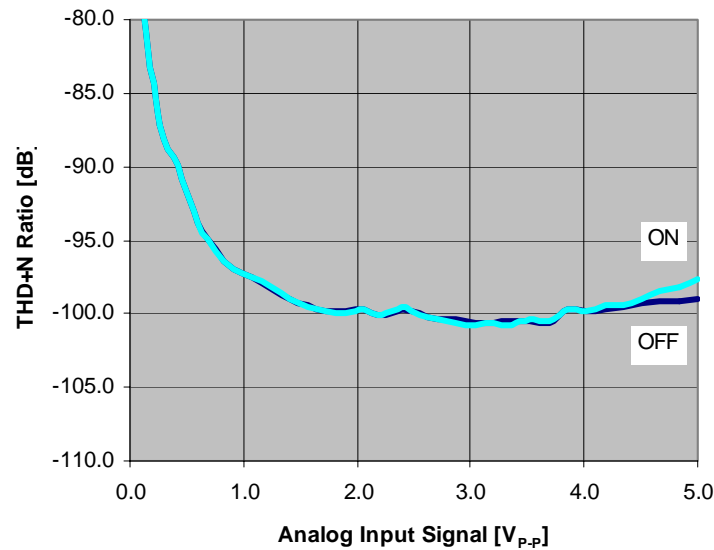
Fig. 7 showed that in differential mode signals applied to the inputs are half the amplitude of the signal applied in single-ended mode. If the common-mode voltage equals the reference voltage, or 2.5 V, the signals in differential mode will swing from 1.25 V to 3.75 V ( $\pm 1.25V$ ). This allows the input FETs to have minimum and constant resistance. To verify this improvement the circuit in Fig. 12 was used for the measurement.



**Fig. 12: Measurement of Differential Input**

As previously, the input signal frequency was set to 100 kHz. As the input signal is differential, the voltage was changed from 0.1 V<sub>p-p</sub> up to 5 V<sub>p-p</sub> as the difference between two signals. This gives us a full-scale measurement range of the ADC, as in previous measurements. The input resistors were set to 100  $\Omega$ , which is comparable to the

200  $\Omega$  in the single-ended mode. Measurements were done for both conversion and sampling modes, or with the input analog switch in both an ON and OFF state (Fig. 13).



**Fig. 13: Distortion At ADC Differential Input Pins In Sampling Mode**

As expected from the previous analysis, the results for an applied differential signal are superior compared to single-ended. Gains of almost 20 dB in THD performance were easily achieved. With differential the inputs do not exceed the linear region of the input FETs so the resistance of the input buffer in front of the ADC has no negative effect on the quality of the signal ADC. This resistor, in combination with the input capacitors, will create an input low-pass filter, additionally reducing the noise coming into the ADC.

## Conclusions

The analog input of the typical SAR ADC is a nonlinear load. This load is both voltage- and frequency-dependent and its biggest influence on an input buffer is when the ADC is in sampling mode. The quality of the input analog signal will be a result of the interaction of the input buffer and the ADC analog input load. Understanding basic processes on the input of the converter can help to keep this problem under control. Applying a differential input signal instead of single-ended signal can lead to improving the THD+N ratio by nearly 20 dB. This improvement is significant for higher frequencies, while for lower frequencies there was not a great influence. Selection of the right configuration and signal level for obtaining maximum performance from the system are dependent on a proper understanding of the internal structure and the interaction between applied components. Using previous analyses and measurement results, a designer can easily maximize performance without incurring additional costs.

## About The Author

Miroslav Oljaca has over 17 years of design and management experience in the field of motor control and power conversion. His design experience ranges from the several watts to the megawatt range. Miroslav currently specifies and supports products that provide motor control solutions targeted at high precision motor control applications. He earned his BSEE and MSEE degrees in electrical engineering at the Electrotechnical University in Belgrade (Yugoslavia). He is a member of the AEI, CNI, IEE and IEEE. He also holds the titles: Eur Ing, Dott.Ing., MSc and CEng. [oljaca\\_miroslav@ti.com](mailto:oljaca_miroslav@ti.com)

